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Test Report issued under the responsibility of:

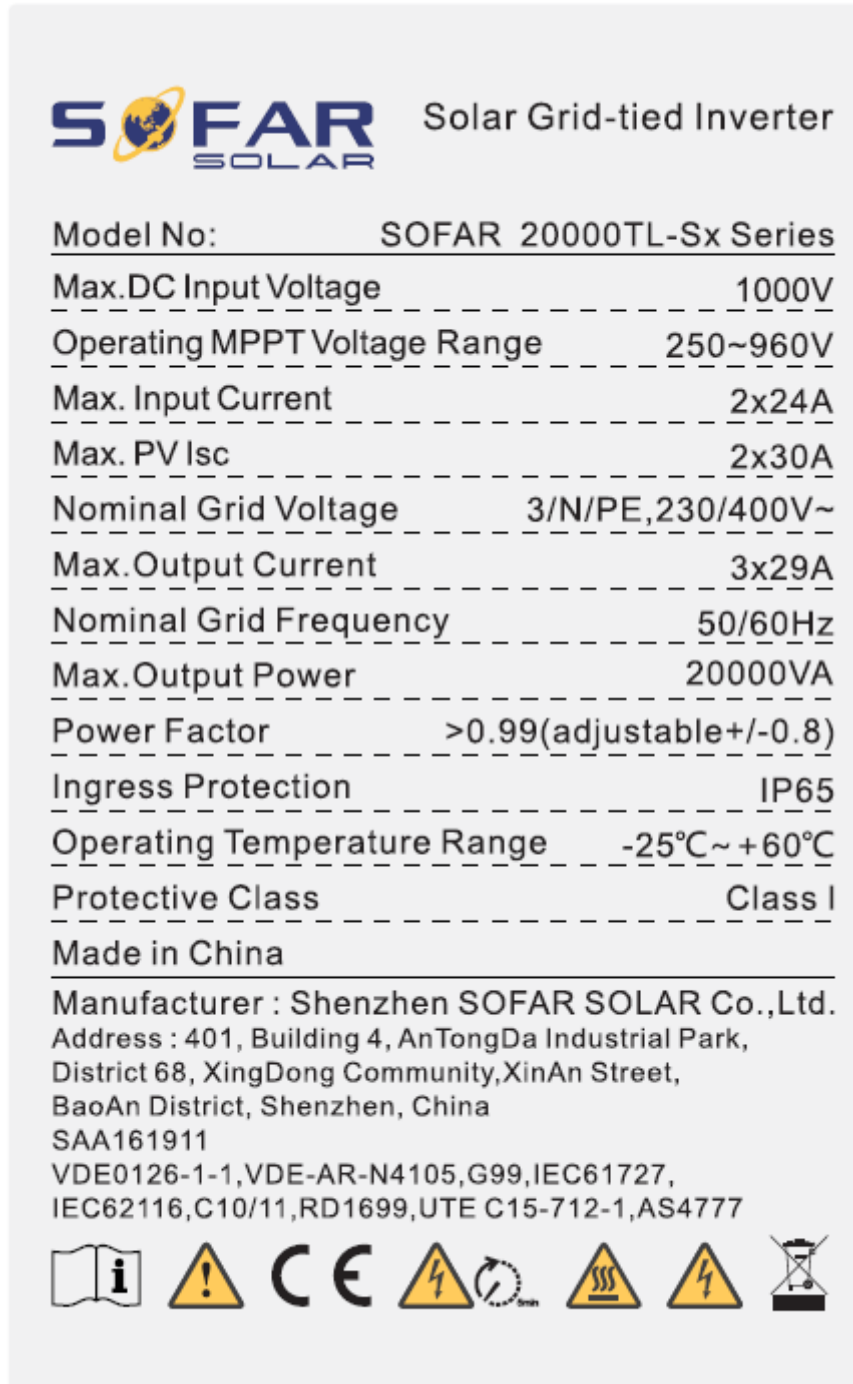


TEST REPORT	
P.O.12.3 Testing of LVRT behaviour	
Requirements for response to voltage dips in wind installations	
Report Reference No	191024045GZU-001
Date of issue	15 Jan 2020
Total number of pages	43 pages
Testing Laboratory	Intertek Testing Services Shenzhen Ltd. Guangzhou Branch
Address	Block E, No.7-2 Guang Dong Software Science Park, Caipin Road, Guangzhou Science City, GETDD, Guangzhou, China
Testing location/ address	Same as above
Tested by (name + signature)	Jason Fu Technical Team Leader
Approved by (+ signature)	Tommy Zhong Technical Manager
Applicant's name	Shenzhen SOFAR SOLAR Co., Ltd.
Address	401, Building 4, AnTongDa Industrial Park, District 68, XingDong Community, XinAn Street, BaoAn District, Shenzhen, China
Test specification:	
Standard	BOE 254:2006 ANNEX P.O.12.3
Test procedure	Type approval
Non-standard test method	N/A
Test Report Form No.	P.O.12.3a
Test Report Form(s) Originator	Intertek Guangzhou
Master TRF	Dated 2019-11
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Test item description	Solar Grid-tied Inverter
Trade Mark	 
Manufacturer	Same as Applicant
Model/Type reference	SOFAR 2000TL-Sx Series, SOFAR 17000TL-Sx Series, SOFAR 15000TL-Sx Series, SOFAR 10000TL-Sx Series (x=0-6)

Ratings	Maximum d.c. input voltage: 1000 V Input voltage rang: 250-960 V Max. input current: 2x24 A (for SOFAR 20000TL-Sx Series); 2x21 A (for SOFAR 17000TL-Sx Series, SOFAR 15000TL-Sx Series); 2x15 A (for SOFAR 10000TL-Sx Series) Max. PV Isc: 2x30 A (for SOFAR 20000TL-Sx Series); 2x27 A (for SOFAR 17000TL-Sx Series, SOFAR 15000TL-Sx Series); 2x20 A (for SOFAR 10000TL-Sx Series) Nominal output voltage: 3/N/PE230V/400V Max. output current: 3x29 A (for SOFAR 20000TL-Sx Series); 3x25 A (for SOFAR 17000TL-Sx Series); 3x22 A (for SOFAR 15000TL-Sx Series); 3x15 A (for SOFAR 10000TL-Sx Series) Nominal frequency: 50 Hz Max. output power: 20000 VA (for 20000TL-Sx Serie); 17000 VA (for SOFAR 17000TL-Sx Serie); 15000 VA (for SOFAR 15000TL-Sx Serie); 10000 VA (for SOFAR 10000TL-Sx Serie) Ingress protection: IP65 Operating temperature range: -25~60°C Software Version: V4.90
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Summary of testing:	
Tests performed (name of test and test clause): All applicable tests The model SOFAR 20000TL-Sx is type tested.	Testing location: Intertek Testing Services Shenzhen Ltd. Guangzhou Branch Block E, No.7-2 Guang Dong Software Science Park, Caipin Road, Guangzhou Science City, GETDD, Guangzhou, China

Copy of marking plate



Note:

1. The above markings are the minimum requirements required by the safety standard. For the final production samples, the additional markings which do not give rise to misunderstanding may be added.
2. Label is attached on the side surface of enclosure and visible after installation
3. The other model labels are identical with label above, except the model name and rating.

<p>Test item particulars</p> <p>Temperature range</p> <p>AC Overvoltage category: <input type="checkbox"/> OVC I <input type="checkbox"/> OVC II <input checked="" type="checkbox"/> OVC III <input type="checkbox"/> OVC IV</p> <p>DC Overvoltage category.....: <input type="checkbox"/> OVC I <input checked="" type="checkbox"/> OVC II <input type="checkbox"/> OVC III <input type="checkbox"/> OVC IV</p> <p>IP protection class</p>
<p>Possible test case verdicts:</p> <p>- test case does not apply to the test object : N/A (Not applicable)</p> <p>- test object does meet the requirement..... : P (Pass)</p> <p>- test object does not meet the requirement..... : F (Fail)</p>
<p>Testing</p> <p>Date of receipt of test item : 01 Dec 2019</p> <p>Date (s) of performance of tests : 01 Dec 2019 – 14 Jan 2020</p>
<p>General remarks:</p> <p>The test results presented in this report relate only to the object tested. This report shall not be reproduced, except in full, without the written approval of the Issuing testing laboratory. "(see Enclosure #)" refers to additional information appended to the report. "(see appended table)" refers to a table appended to the report.</p> <p>When determining for test conclusion, measurement uncertainty of tests has been considered. This report is for the exclusive use of Intertek's Client and is provided pursuant to the agreement between Intertek and its Client. Intertek's responsibility and liability are limited to the terms and conditions of the agreement. Intertek assumes no liability to any party, other than to the Client in accordance with the agreement, for any loss, expense or damage occasioned by the use of this report. Only the Client is authorized to permit copying or distribution of this report and then only in its entirety. Any use of the Intertek name or one of its marks for the sale or advertisement of the tested material, product or service must first be approved in writing by Intertek. The observations and test results in this report are relevant only to the sample tested. This report by itself does not imply that the material, product, or service is or has ever been under an Intertek certification program. The test report only allows to be revised only within the report defined retention period unless standard or regulation was withdrawn or invalid.</p> <p>Throughout this report a point is used as the decimal separator.</p> <p>Description of the vector system to depict test result:</p> <p>The regarded system of the voltage and current vectors is the generator reference system:</p> <ul style="list-style-type: none"> ● If the inverter feeds to the grid the active power is measured with positive sign ● If the inverter generates inductive reactive power the reactive power has a positive sign ● If the inverter generates capacitive reactive power the reactive power has a negative sign <p>Factory information: Dongguan SOFAR SOLAR Co., Ltd 1F-6F, Building E, No.1 JinQi Road, Bihu Industrial Park, Wulian Village, Fenggang Town, Dongguan City</p>

General product information:

The unit is a three-phase solar inverter, it can convert the high PV voltage to AC output.

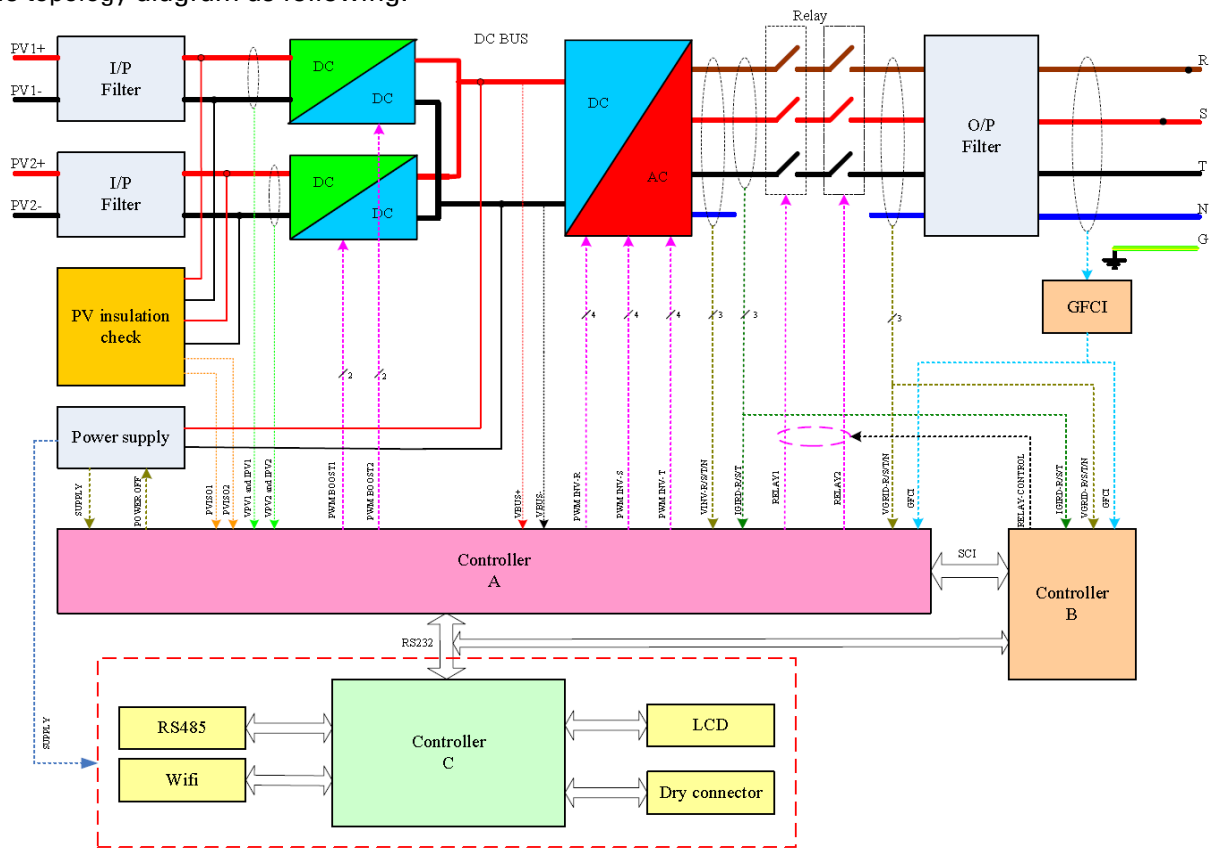
The unit is providing EMI filtering at the PV. It does not provide basic insulation separate from PV side to Grid (transformerless).

The unit has two controllers. the master controller A monitor the PV statue; measure the PV voltage and current, bus voltage, AC voltage, current, GFCI and frequency.

The slave controller B monitor AC voltage, GFCI and communicate with the master controller A

The master controller A and controller B are used together to control relay open or close, if the single fault on one MCU, the other one MUC can be capable to open the relay, so that still providing safety means

The topology diagram as following:



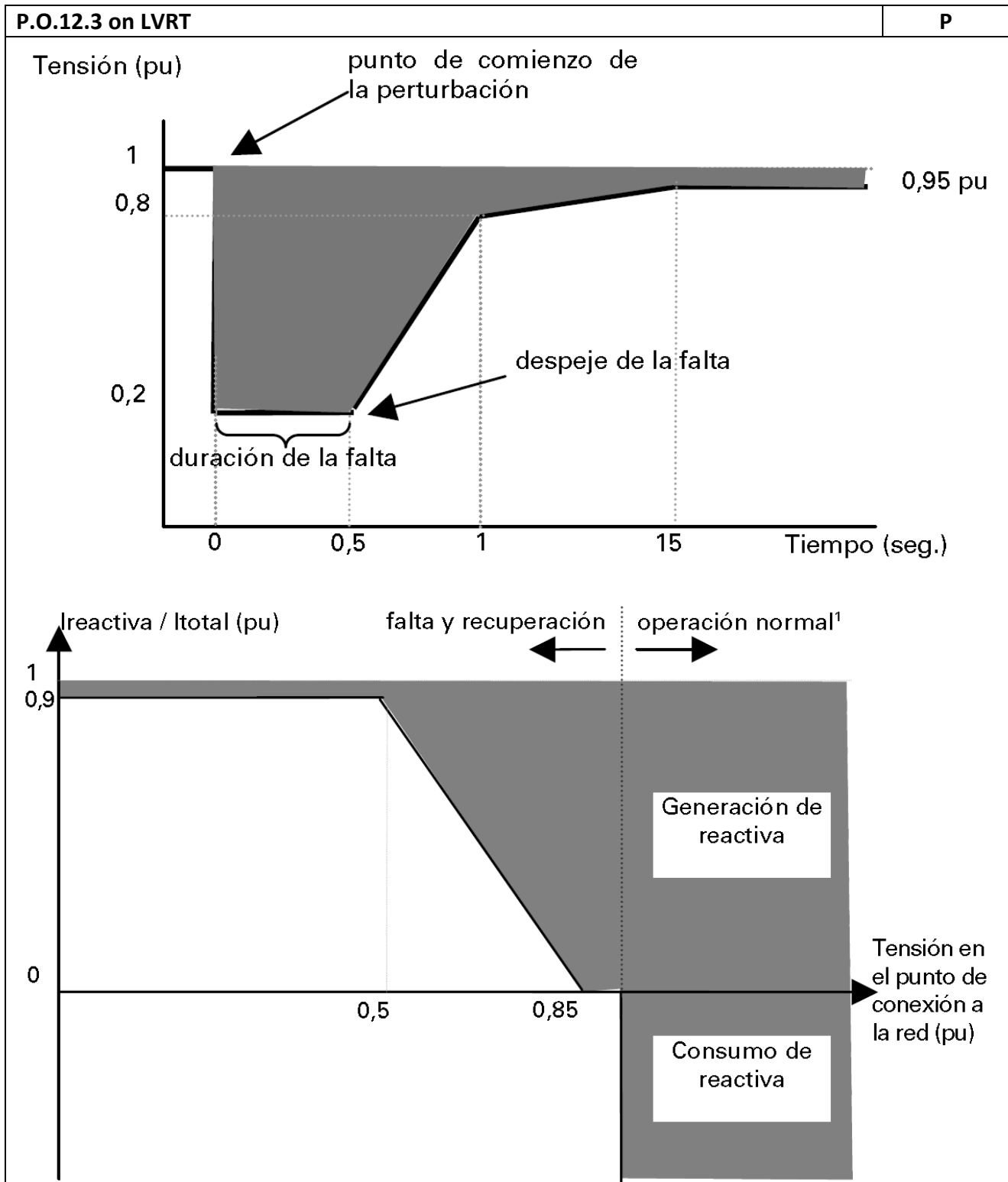
Model differences:

All models have identical mechanical and electrical construction except some parameter of the software architecture to control the max output power. The detailed difference as following:

Model	DC Cable Gland	PV connector	DC inside connector	Fuse PCB+ String detection board	DC surge arrester	DC switch	AC switch	AC surge arrester
Sofar 20000TL-S0 Sofar 17000TL-S0 Sofar 15000TL-S0 Sofar 10000TL-S0	√		√					

Sofar 20000TL-S1	√		√			√		
Sofar 17000TL-S1								
Sofar 15000TL-S1								
Sofar 10000TL-S1								
Sofar 20000TL-S2		√	√			√		
Sofar 17000TL-S2								
Sofar 15000TL-S2								
Sofar 10000TL-S2								
Sofar 20000TL-S3		√		√		√		
Sofar 17000TL-S3								
Sofar 15000TL-S3								
Sofar 10000TL-S3								
Sofar 20000TL-S4		√		√	√	√		
Sofar 17000TL-S4								
Sofar 15000TL-S4								
Sofar 10000TL-S4								
Sofar 20000TL-S5		√		√	√	√		√
Sofar 17000TL-S5								
Sofar 15000TL-S5								
Sofar 10000TL-S5								
Sofar 20000TL-S6		√		√	√	√	√	√
Sofar 17000TL-S6								
Sofar 15000TL-S6								
Sofar 10000TL-S6								
√ denote incorporating this component								

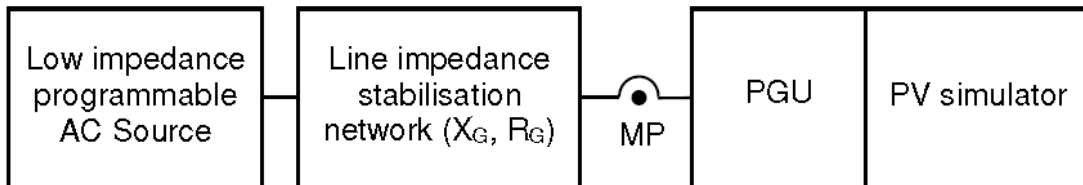
Appended Table - Testing Result:



Behaviour during grid disturbance							
No. load Test	No. of phase					Test number	
1	Three					1.1	
	Two					1.2A (for test A) 1.2B (for test B) 1.2C (for test C)	
	One					1.3A(for test A) 1.3B(for test B) 1.3C(for test A)	
No. load Test	No. of phase	Output power level			Duration of voltage dip	Test number	Verdict
Three-phase system							
2	Three	P>0.8Pn	100%	Ures<20%Un	t>500ms	2.1	P
		0.1Pn<P<0.3Pn	20%			2.2	P
	Two	P>0.8Pn	100%	Ures<60%Un	t>750ms	2.3	P
		0.1Pn<P<0.3Pn	20%			2.4	P
	One	P>0.8Pn	100%	Ures<60%Un	t>750ms	2.5	P
		0.1Pn<P<0.3Pn	20%			2.6	P
Single-phase system							
3	One	P>0.8Pn	100%	Ures<20%Un	t>500ms	3.1	N/A
		0.1Pn<P<0.3Pn	20%			3.2	N/A
		P>0.8Pn	100%	Ures<60%Un	t>750ms	3.3	N/A
		0.1Pn<P<0.3Pn	20%			3.4	N/A

Behaviour during grid disturbance

Schematic of test setup:



Note on test setup:

A programmable AC source used.

Note:

Measurement points used: MP

Evaluation of data measured at MP

Used sample rate: 10KHz

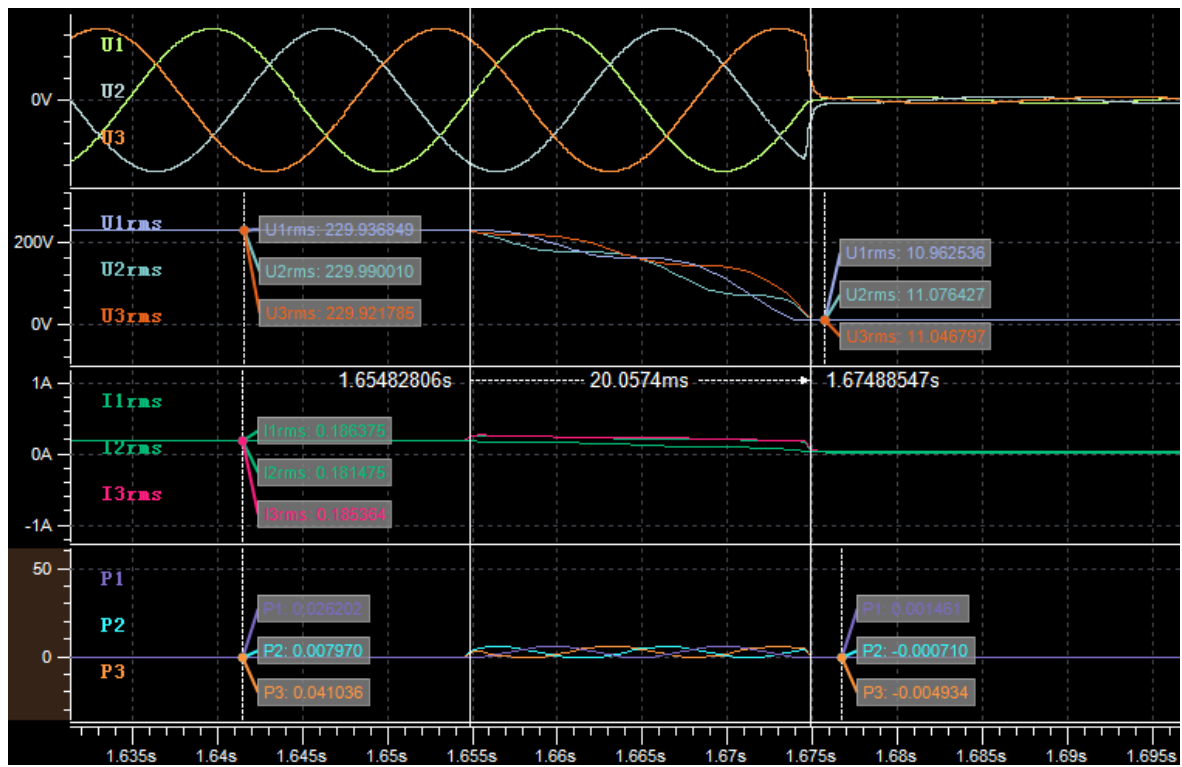
Description of the type of voltage dips:

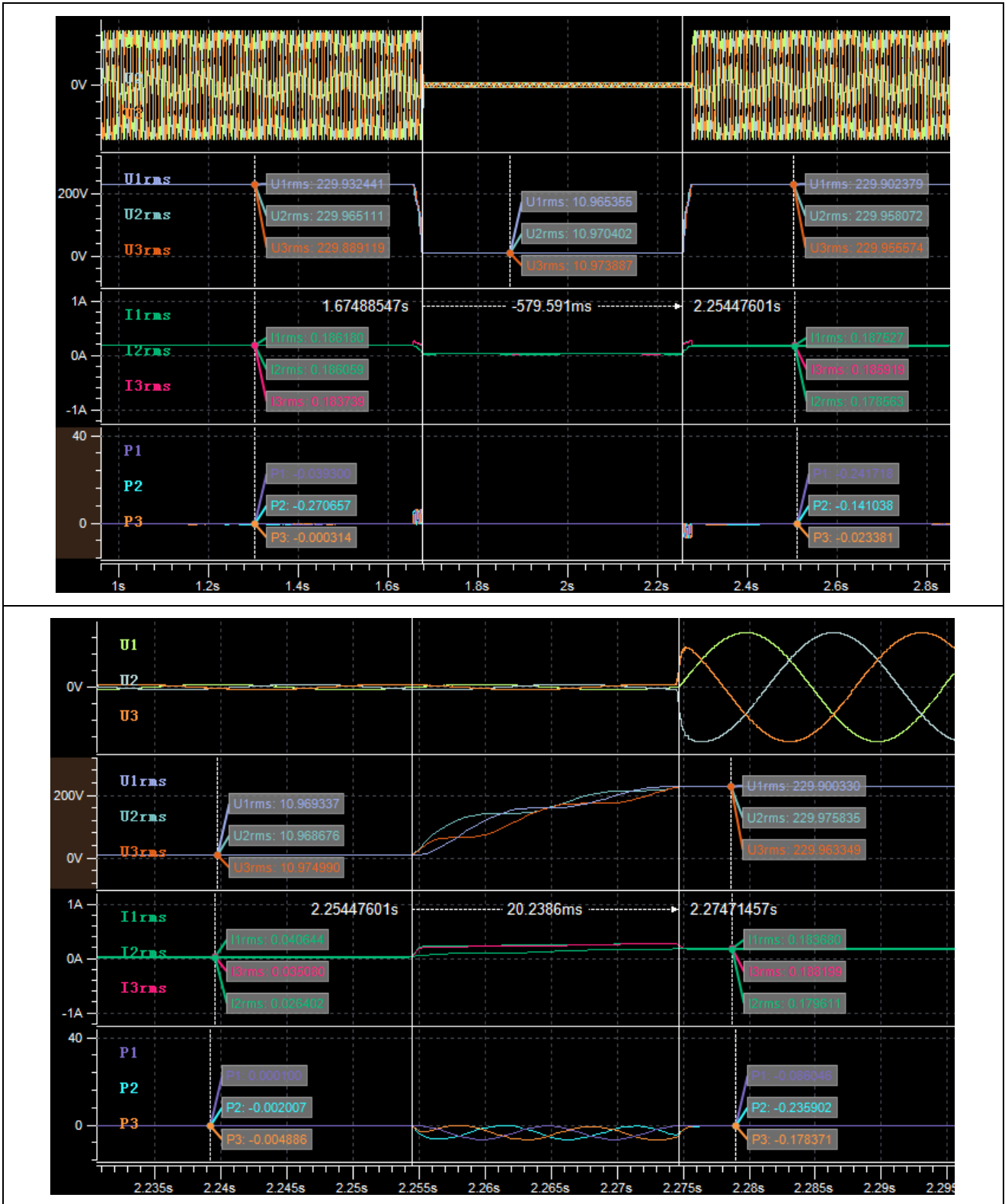
Asymmetric voltage dips were simulated to mirror the behavior during phase to phase faults (isolated) on a medium voltage grid separated by DY5 transformer. Symmetric dips were simulated as three-phase faults (isolated) based on the same setup.

Grid parameters at MP

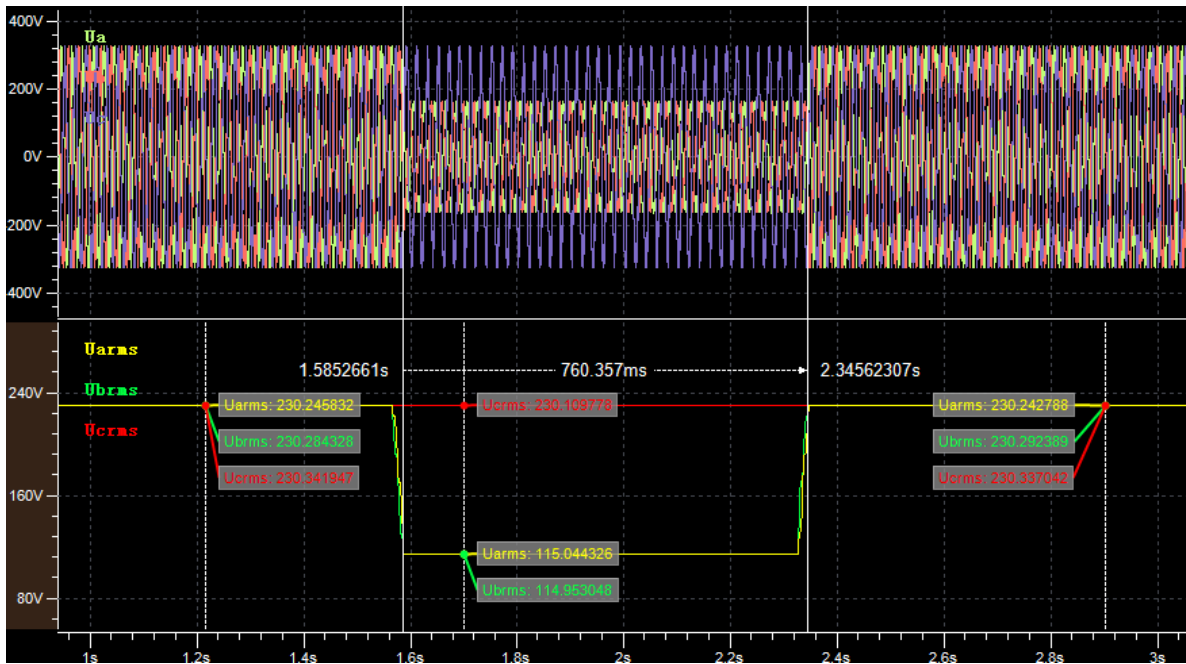
Nominal voltage PCC // U[V]	230Vac (L-N)
Minimal short circuit power // S _K [KVA]	60
Grid impedance R [mΩ]	1.81
Grid reactance X [mΩ]	5.56

Behaviour during grid disturbance			
Test			
Test No.	1.1		
Phase No.	1	2	3
Fault duration [ms]	>500	>500	>500
Voltage $U_{pre-fault}$ [V] (Average of all phase)	229.93		
Residual voltage [V] (Average of all phase)	10.97		
Fault duration [ms]	579.59		

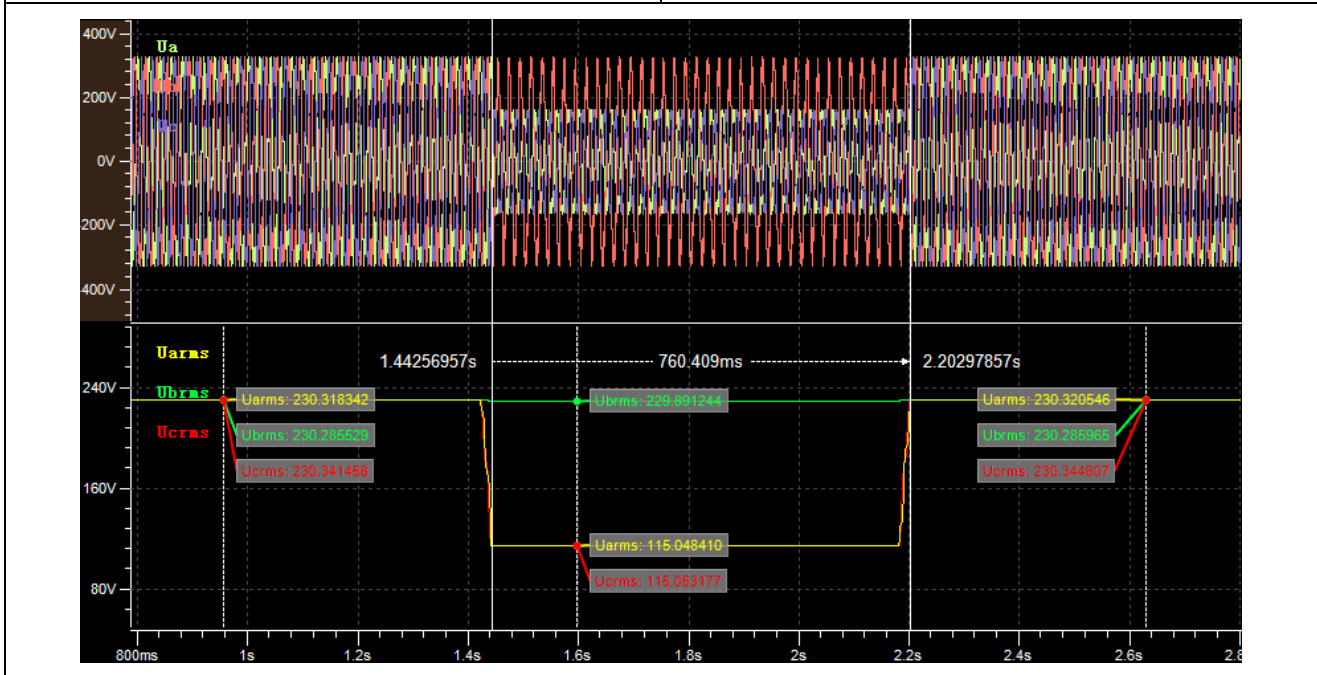




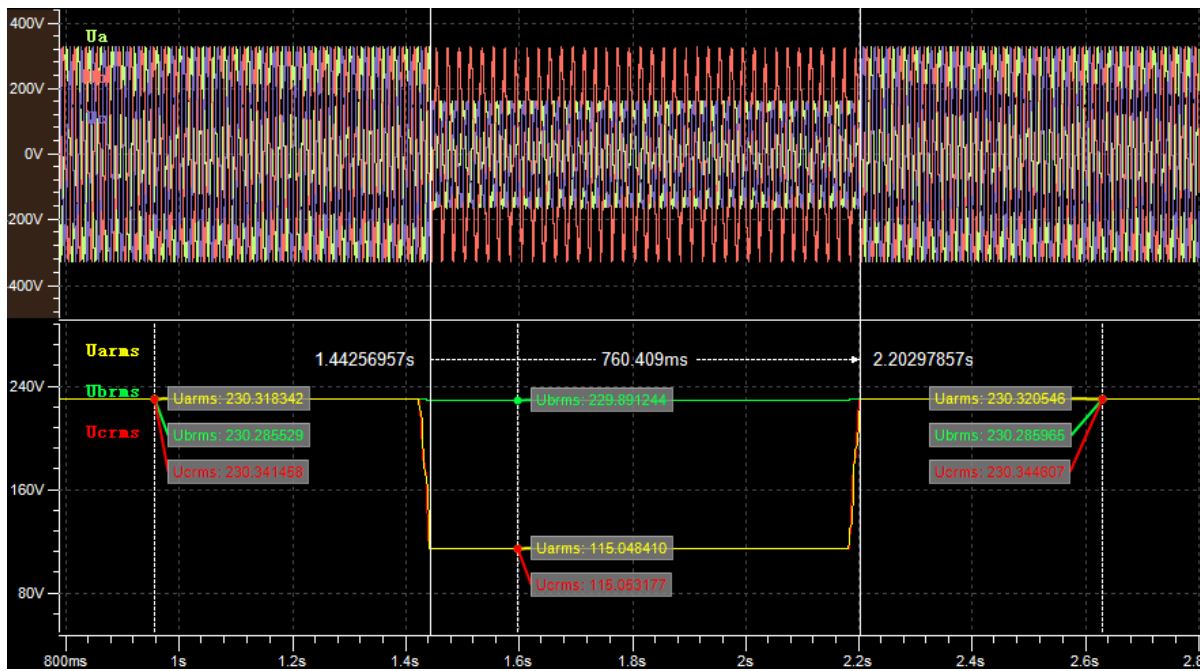
Behaviour during grid disturbance			
Test			
Test No.	1.2A		
Phase No.	1	2	3
Fault duration [ms]	>750	>750	>750
Voltage $U_{pre-fault}$ [V](Average of all phase)	229.93		
Residual voltage [V]	114.79	114.82	229.54
Fault duration [ms]	739		



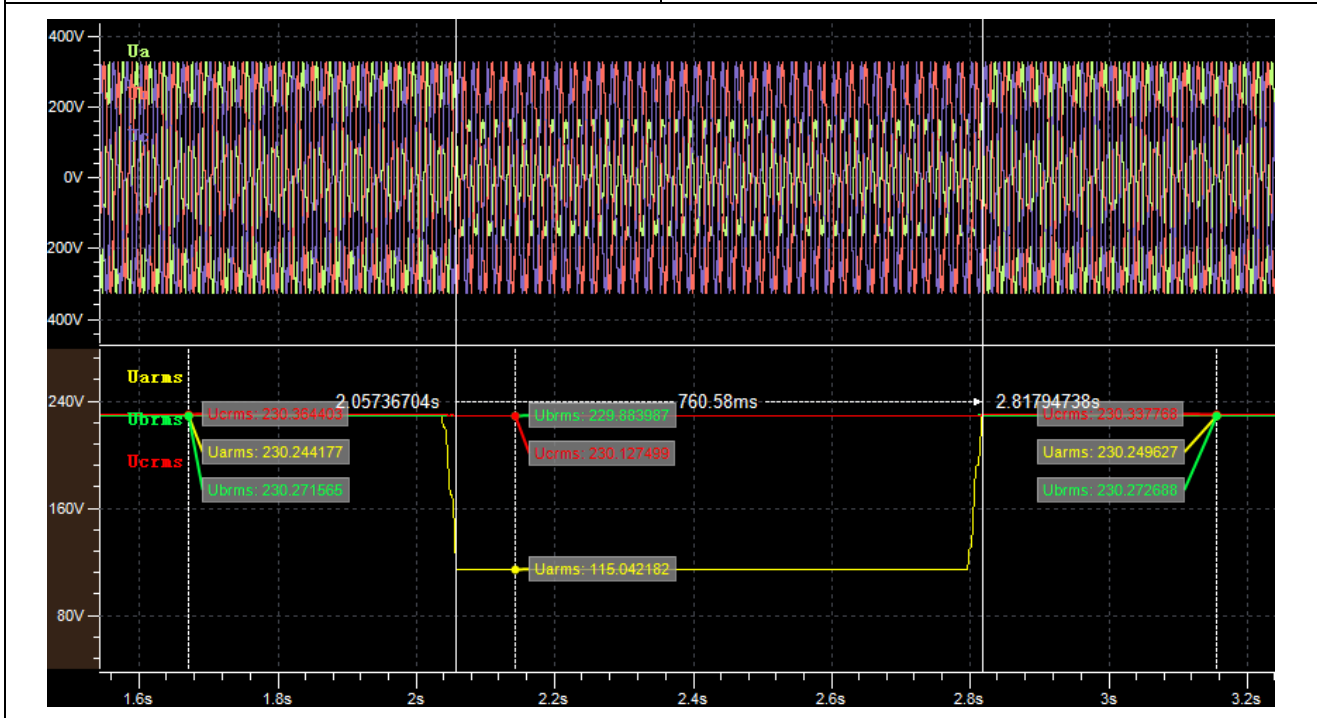
Behaviour during grid disturbance			
Test			
Test No.	1.2B		
Phase No.	1	2	3
Fault duration [ms]	>750	>750	>750
Voltage $U_{pre-fault}$ [V](Average of all phase)	230.31		
Residual voltage [V]	115.04	229.89	115.05
Fault duration [ms]	760.41		



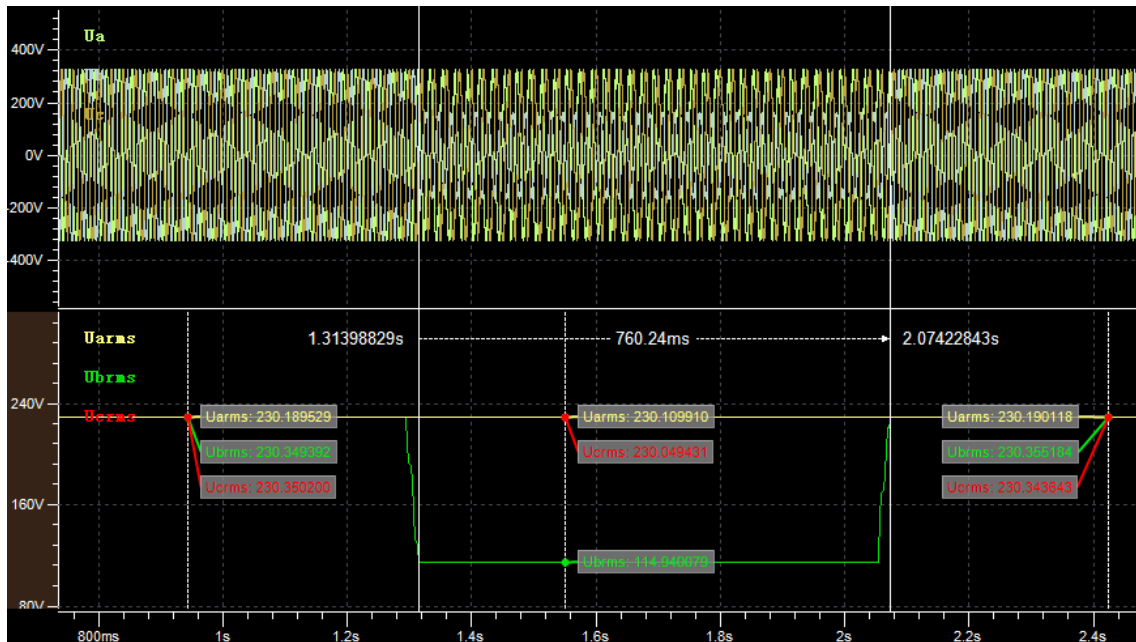
Behaviour during grid disturbance			
Test			
Test No.	1.2C		
Phase No.	1	2	3
Fault duration [ms]	>750	>750	>750
Voltage $U_{pre-fault}$ [V](Average of all phase)	230.22		
Residual voltage [V]	230.04	114.97	115.05
Fault duration [ms]	759.86		



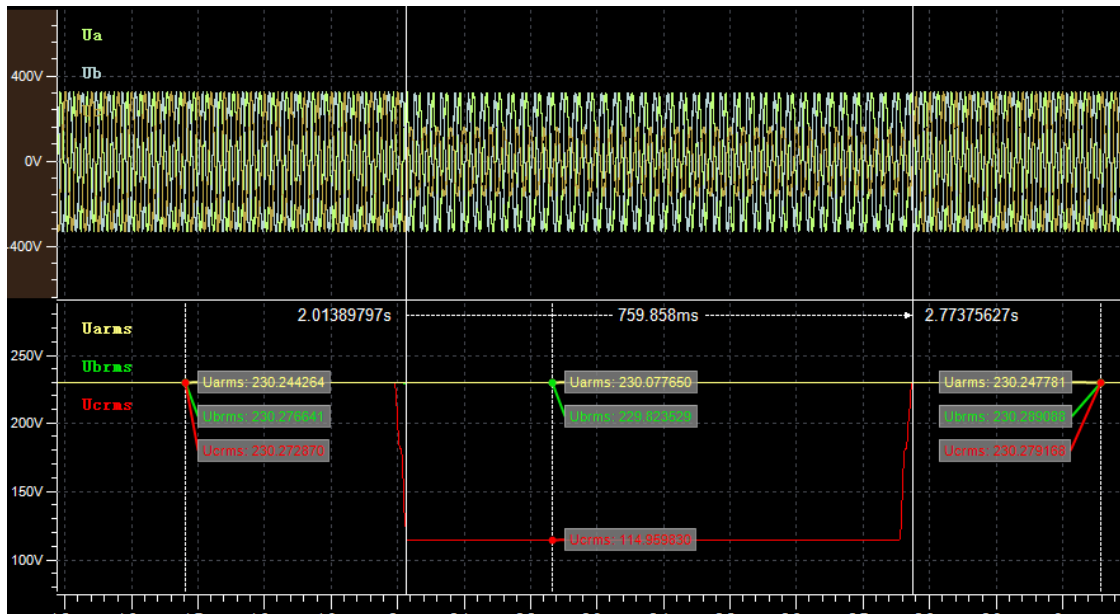
Behaviour during grid disturbance			
Test			
Test No.	1.3A		
Phase No.	1	2	3
Fault duration [ms]	>750	>750	>750
Voltage $U_{pre-fault}$ [V](Average of all phase)	230.24		
Residual voltage [V]	115.04	229.88	230.13
Fault duration [ms]	760.58		



Behaviour during grid disturbance			
Test			
Test No.	1.3B		
Phase No.	1	2	3
Fault duration [ms]	>750	>750	>750
Voltage $U_{pre-fault}$ [V](Average of all phase)	230.29		
Residual voltage [V]	230.11	114.94	230.05
Fault duration [ms]	760.24		

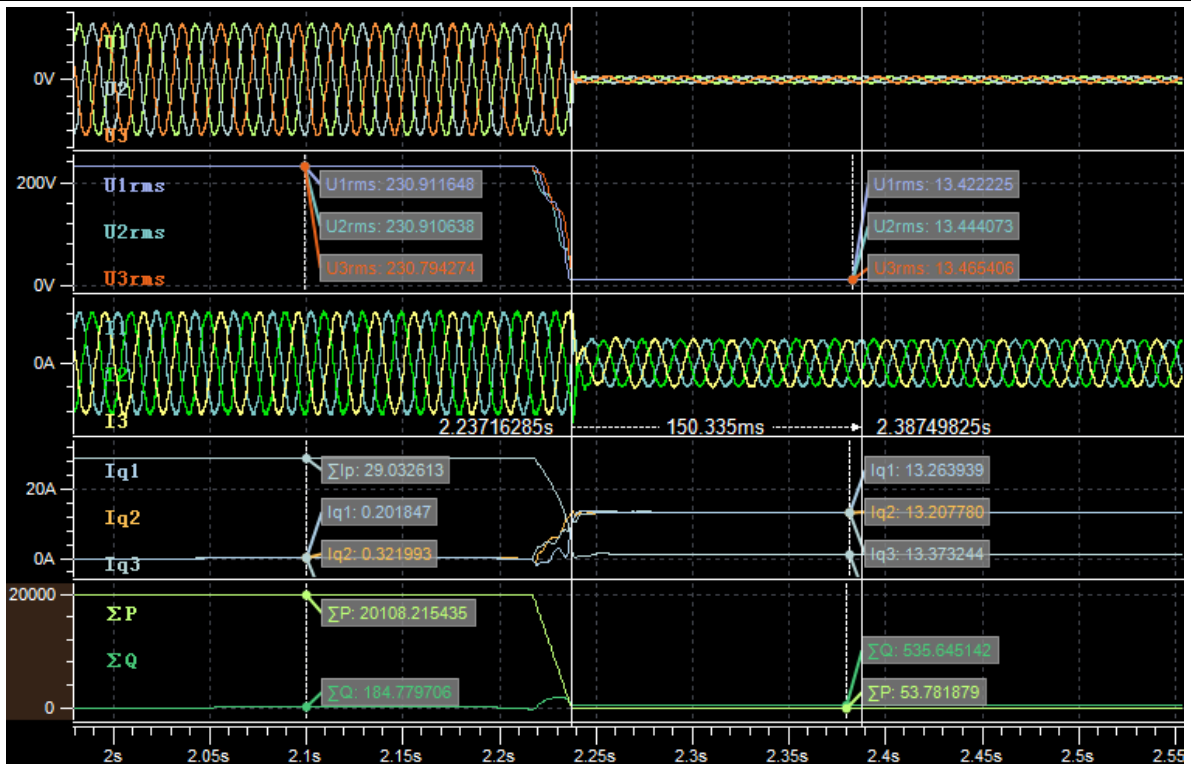


Behaviour during grid disturbance			
Test			
Test No.	1.3C		
Phase No.	1	2	3
Fault duration [ms]	>750	>750	>750
Voltage $U_{pre-fault}$ [V](Average of all phase)	230.26		
Residual voltage [V]	230.08	229.82	114.96
Fault duration [ms]	758.86		

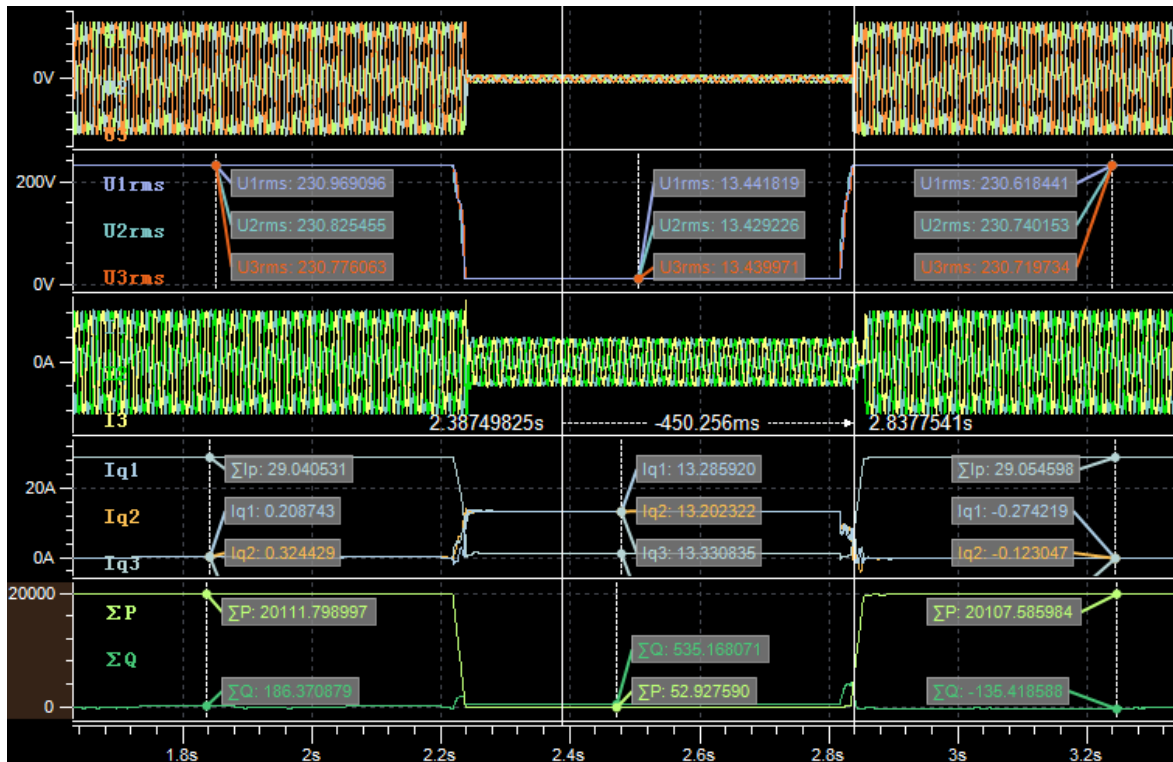


Behaviour during grid disturbance				
Balanced faults				
Test No.2.1				
Voltage dip	Measurement			Limit
	Phase A	Phase B	Phase C	
Voltage dip and during 150ms				
Net consumption $Q < 60\%P_n$ (20ms)	0.027 p.u	0.027 p.u	0.027 p.u	-0.6p.u
Voltage dip after 150ms until recovery				
Net consumption $P < 10\%P_n$ (20ms)	0.0026p.u	0.0026p.u	0.0026p.u	-0.1p,u
Reactive current ratio: $I_{\text{reactive}}/I_{\text{total}}$	0.946 p.u	0.942p.u	0.959p.u	>0.9p.u
Voltage recovery during 150ms				
Net reactive consumption energy $E_r < 60\%P_n * 150\text{ms}$	-1.026 ms*p.u	-2.045 ms*p.u	-5.367 ms*p.u	-90ms*p.u
Net reactive consumption $I_r < 1.5I_n$ (20ms)	-0.009 p.u	-0.005 p.u	-0.036 p.u	-1.5 p.u

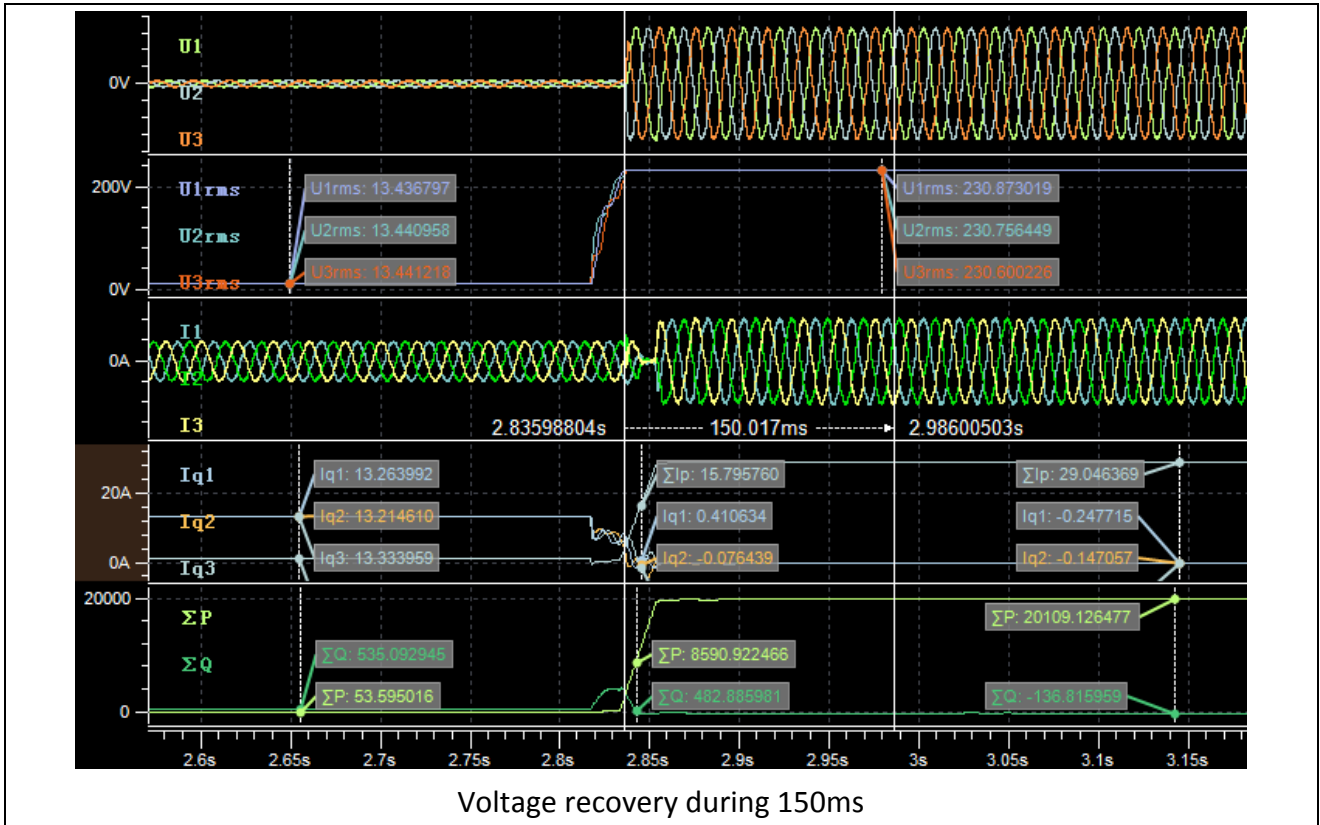
Graph_Phase A



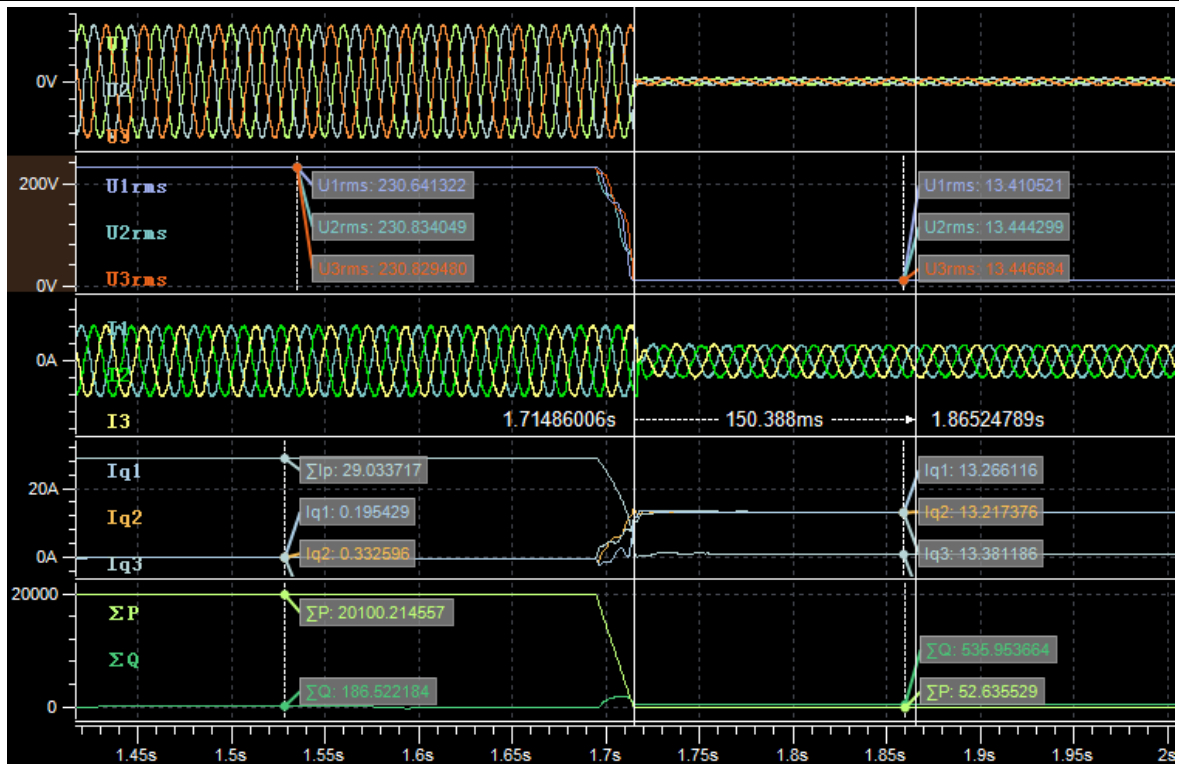
Voltage dip and during 150ms



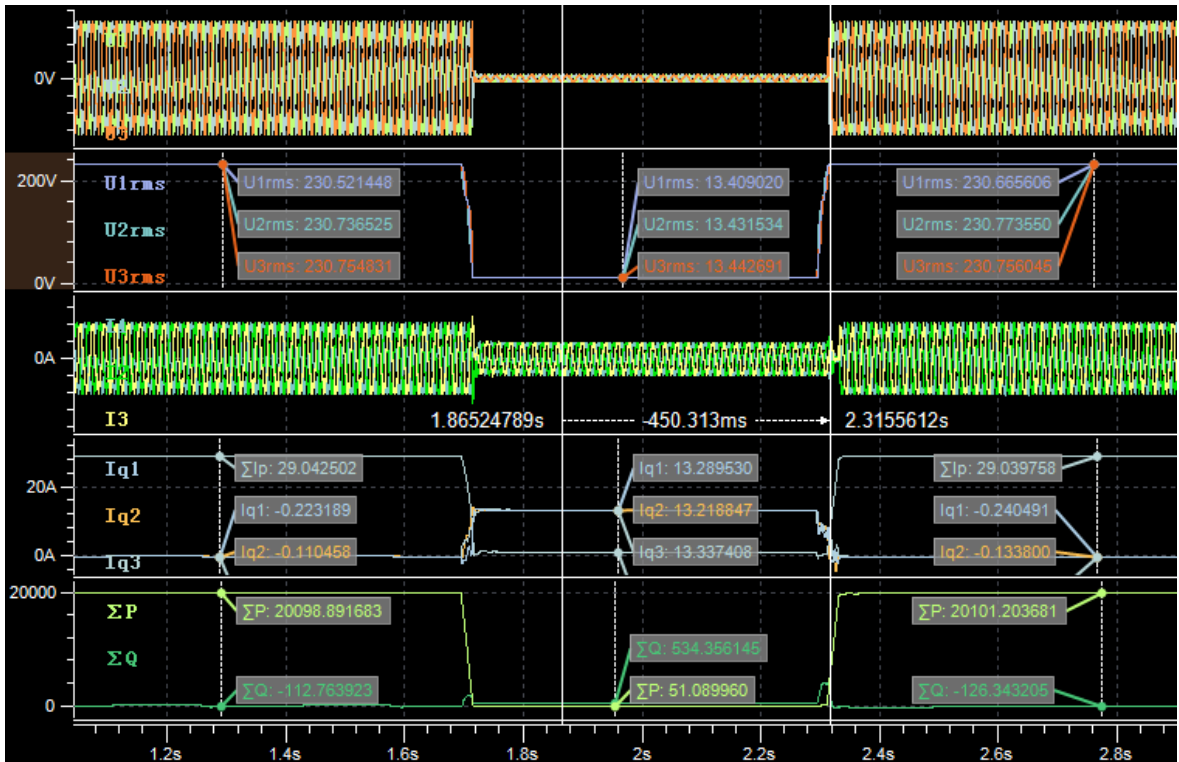
Voltage dip after 150ms until recovery



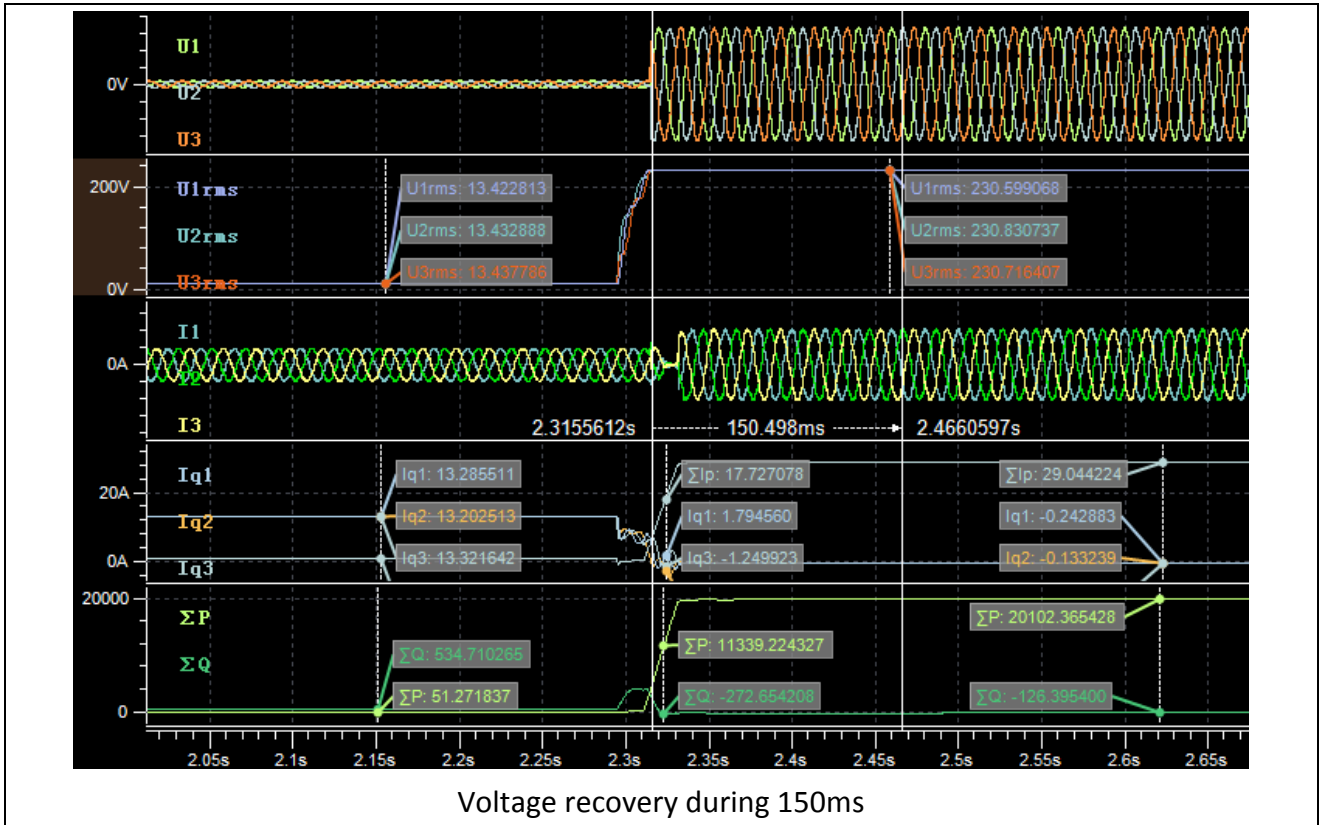
Graph_Phase B



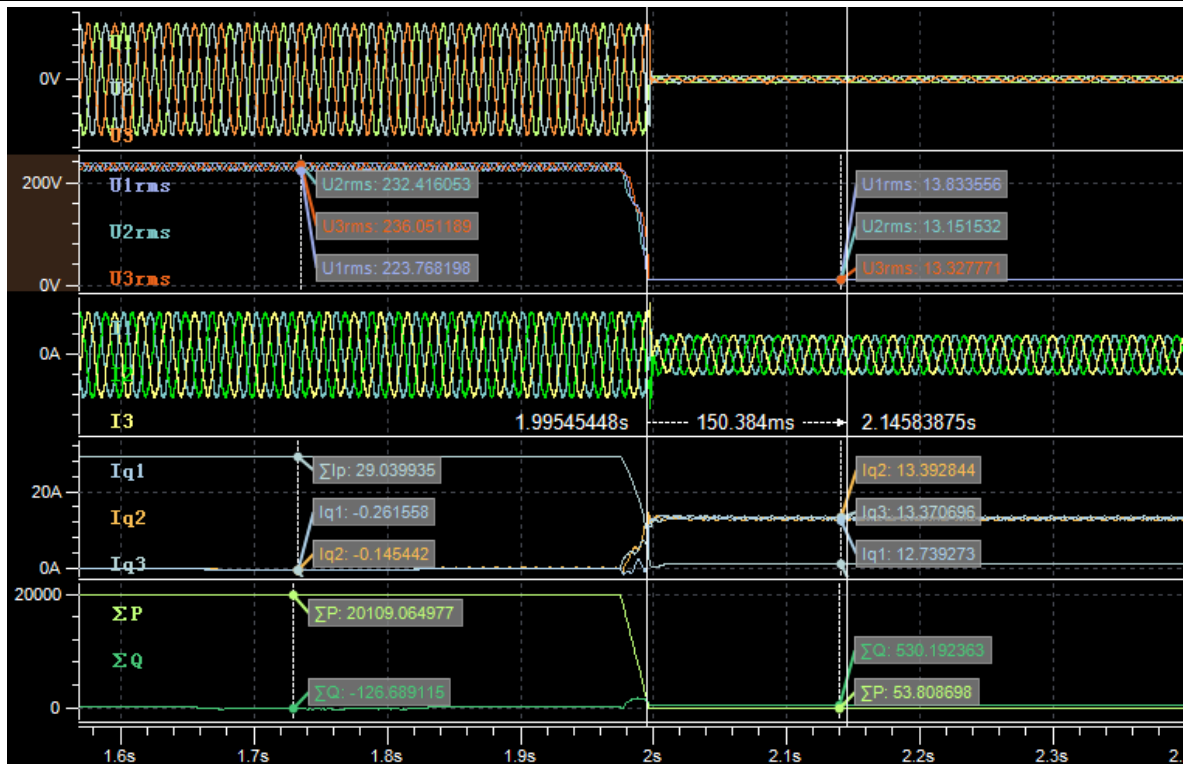
Voltage dip and during 150ms



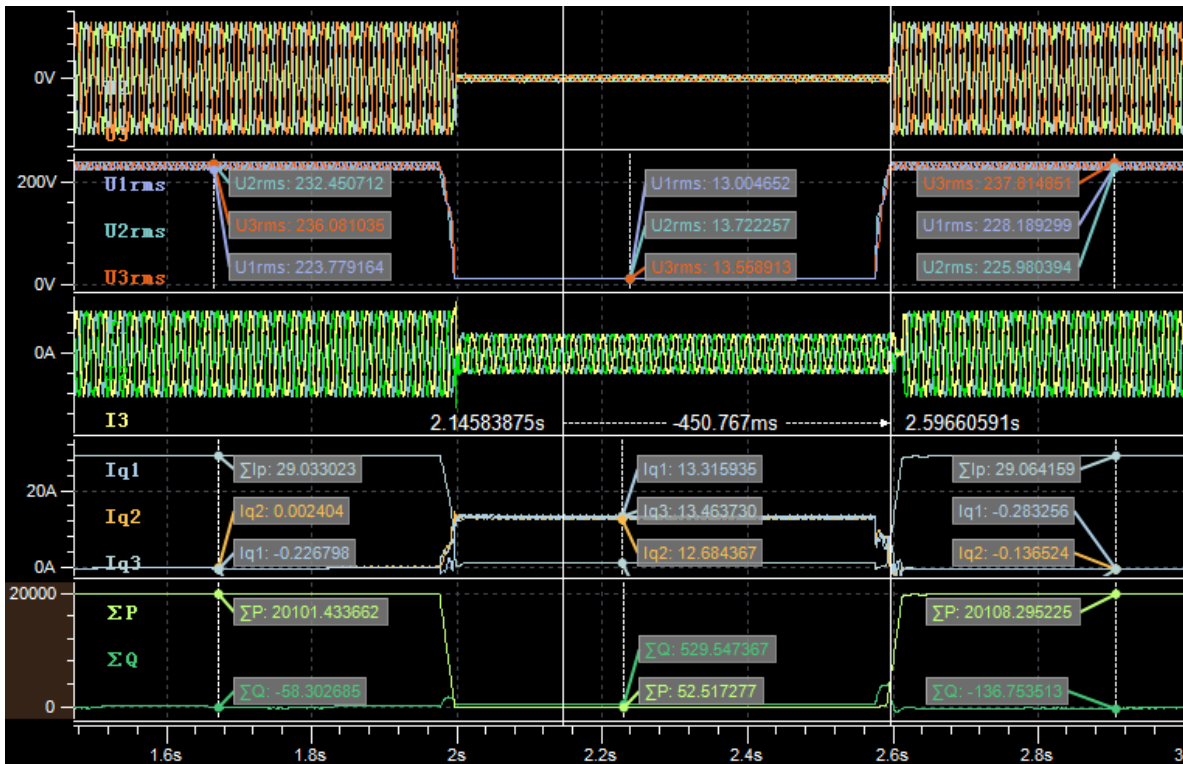
Voltage dip after 150ms until recovery



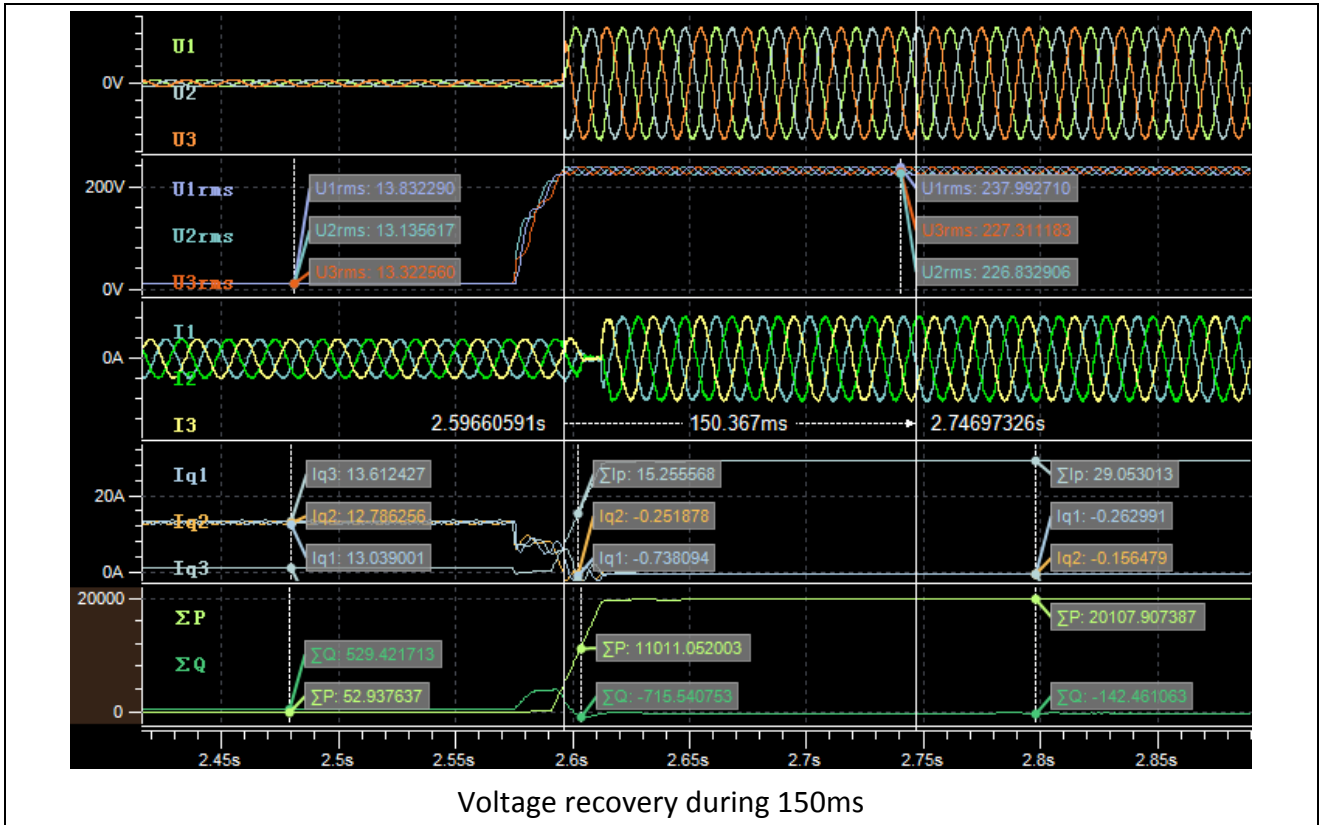
Graph_Phase C



Voltage dip and during 150ms

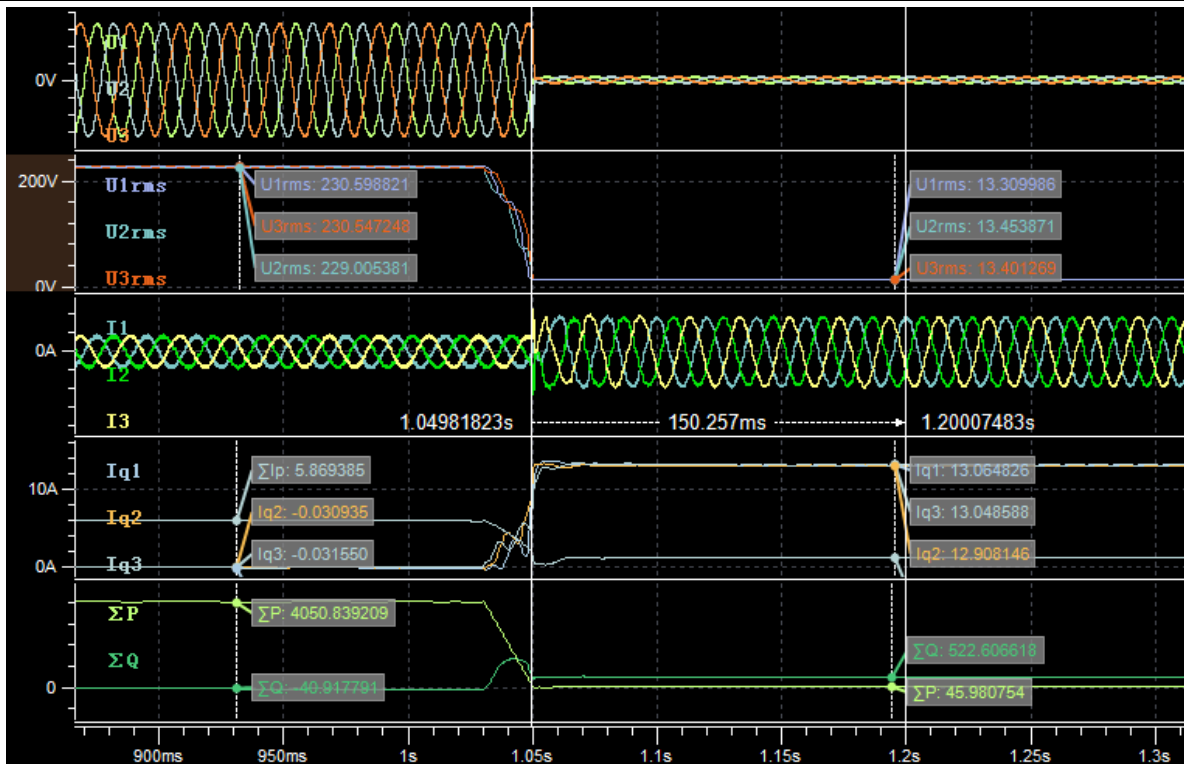


Voltage dip after 150ms until recovery

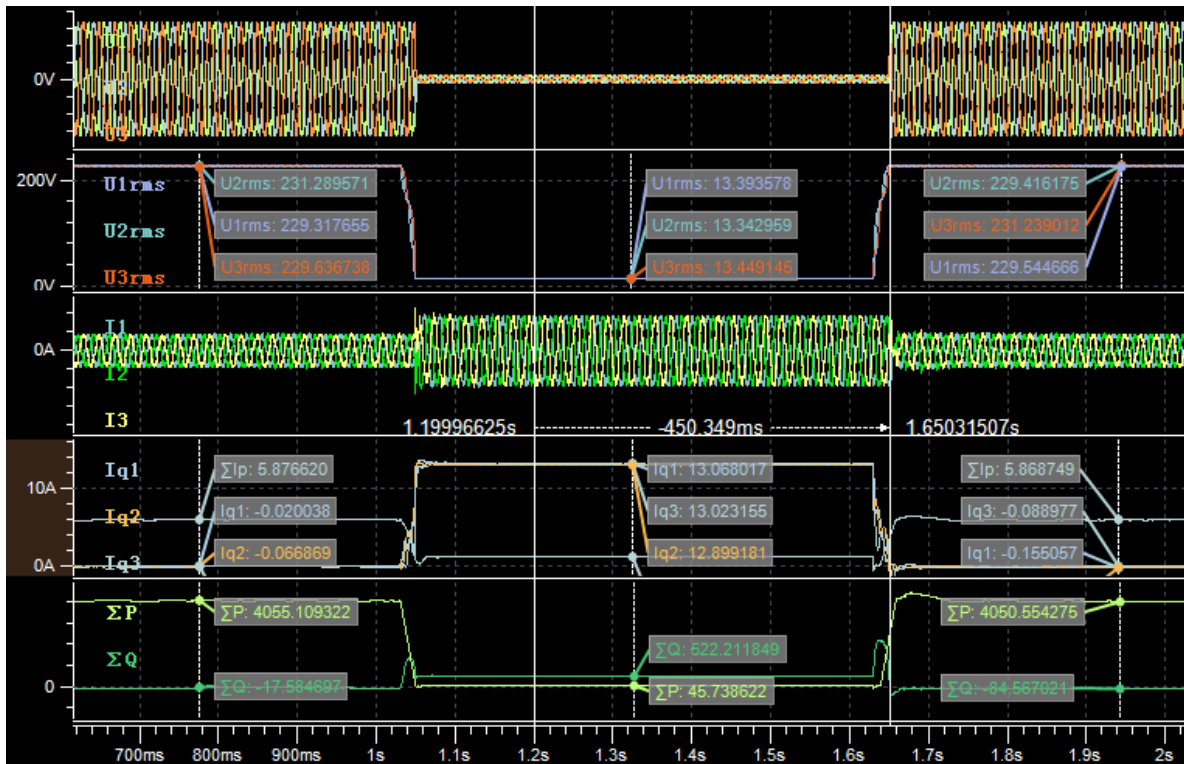


Behaviour during grid disturbance				
Balanced faults				
Test No.2.2				
Voltage dip	Measurement			Limit
	Phase A	Phase B	Phase C	
Voltage dip and during 150ms				
Net consumption $Q < 60\%P_n$ (20ms)	0.026 p.u	0.026 p.u	0.027 p.u	-0.6p.u
Voltage dip after 150ms until recovery				
Net consumption $P < 10\%P_n$ (20ms)	0.0023p.u	0.0022p.u	0.0024p.u	-0.1p,u
Reactive current ratio: $I_{reactive}/I_{total}$	0.931 p.u	0.922p.u	0.950p.u	>0.9p.u
Voltage recovery during 150ms				
Net reactive consumption energy $E_r < 60\%P_n * 150ms$	-2.015 ms*p.u	-3.076 ms*p.u	-0.601 ms*p.u	-90ms*p.u
Net reactive consumption $I_r < 1.5I_n$ (20ms)	-0.013 p.u	-0.018 p.u	-0.003 p.u	-1.5 p.u

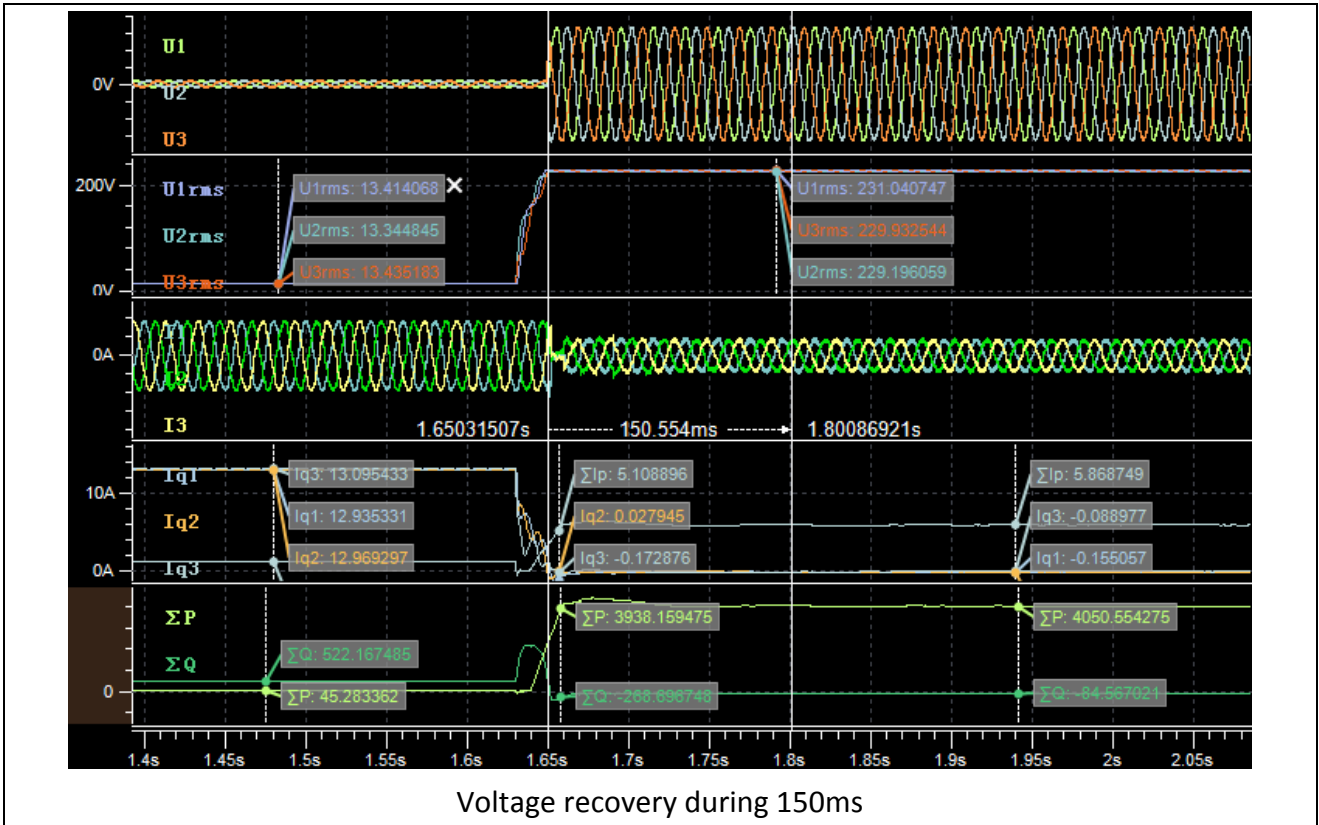
Graph_Phase A



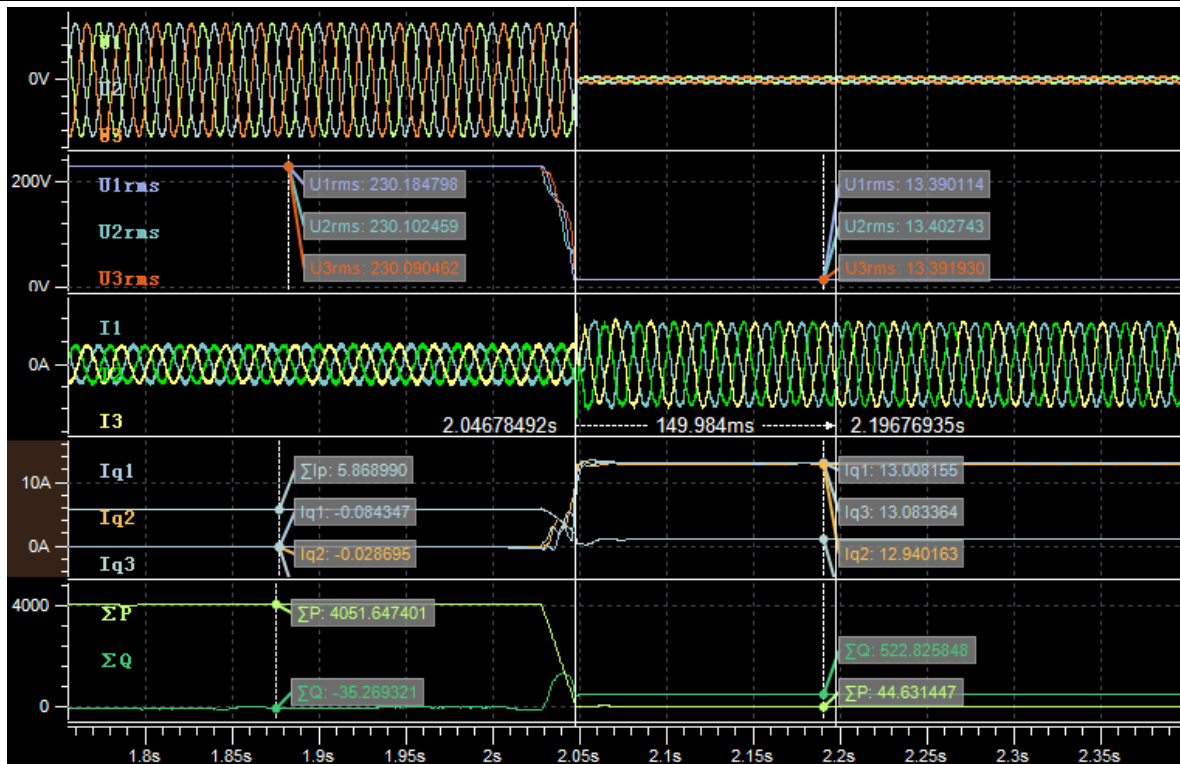
Voltage dip and during 150ms



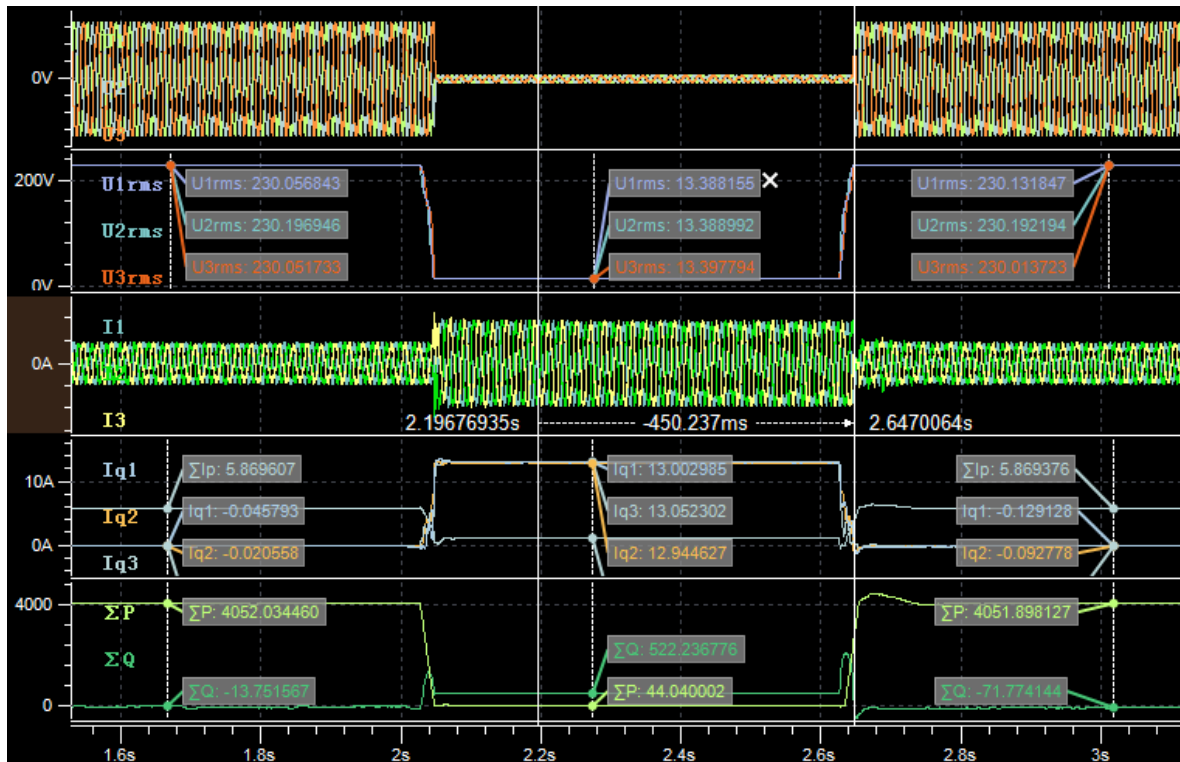
Voltage dip after 150ms until recovery



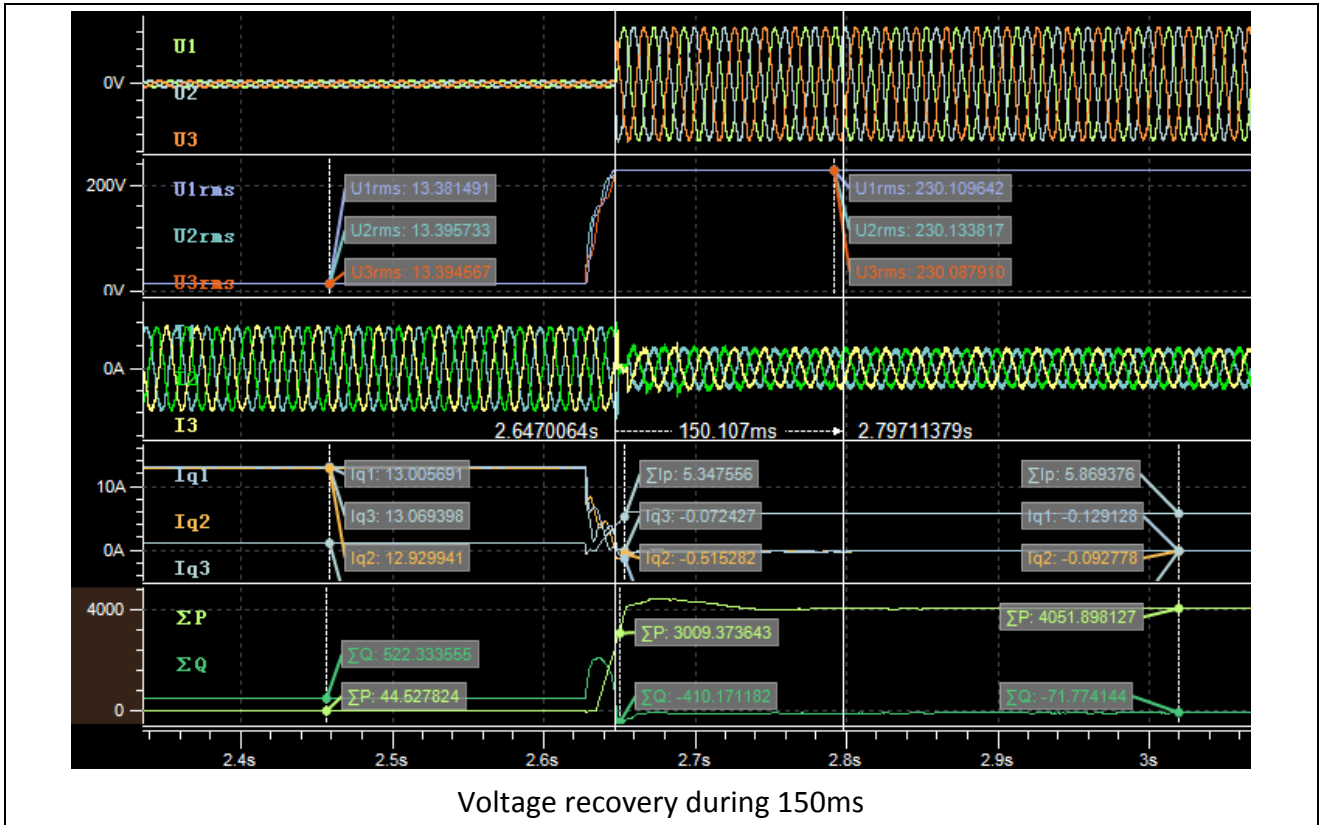
Graph_Phase B



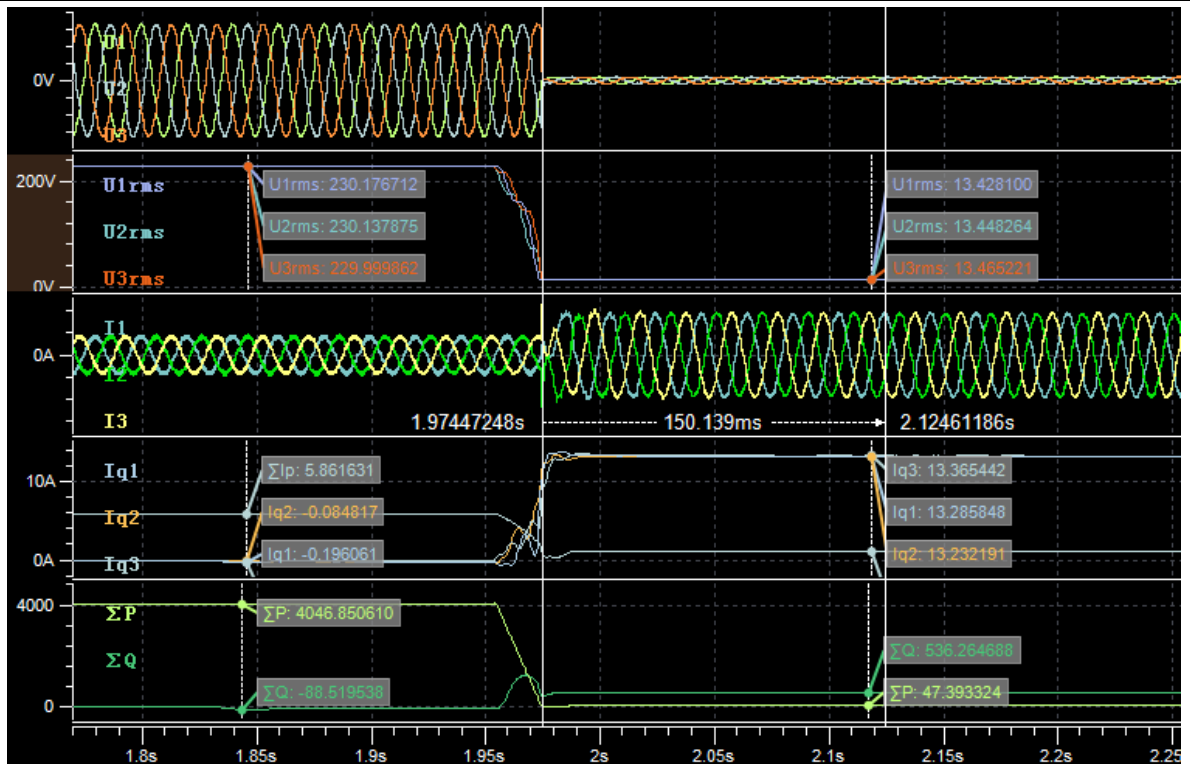
Voltage dip and during 150ms



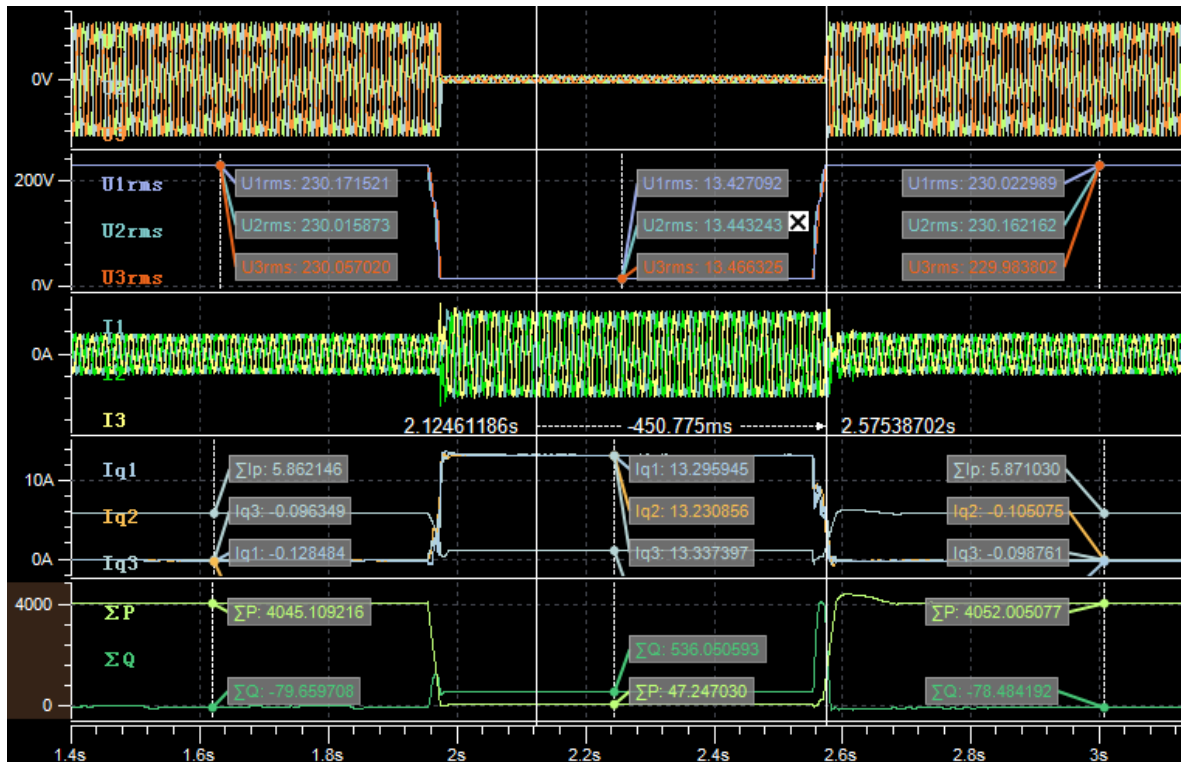
Voltage dip after 150ms until recovery



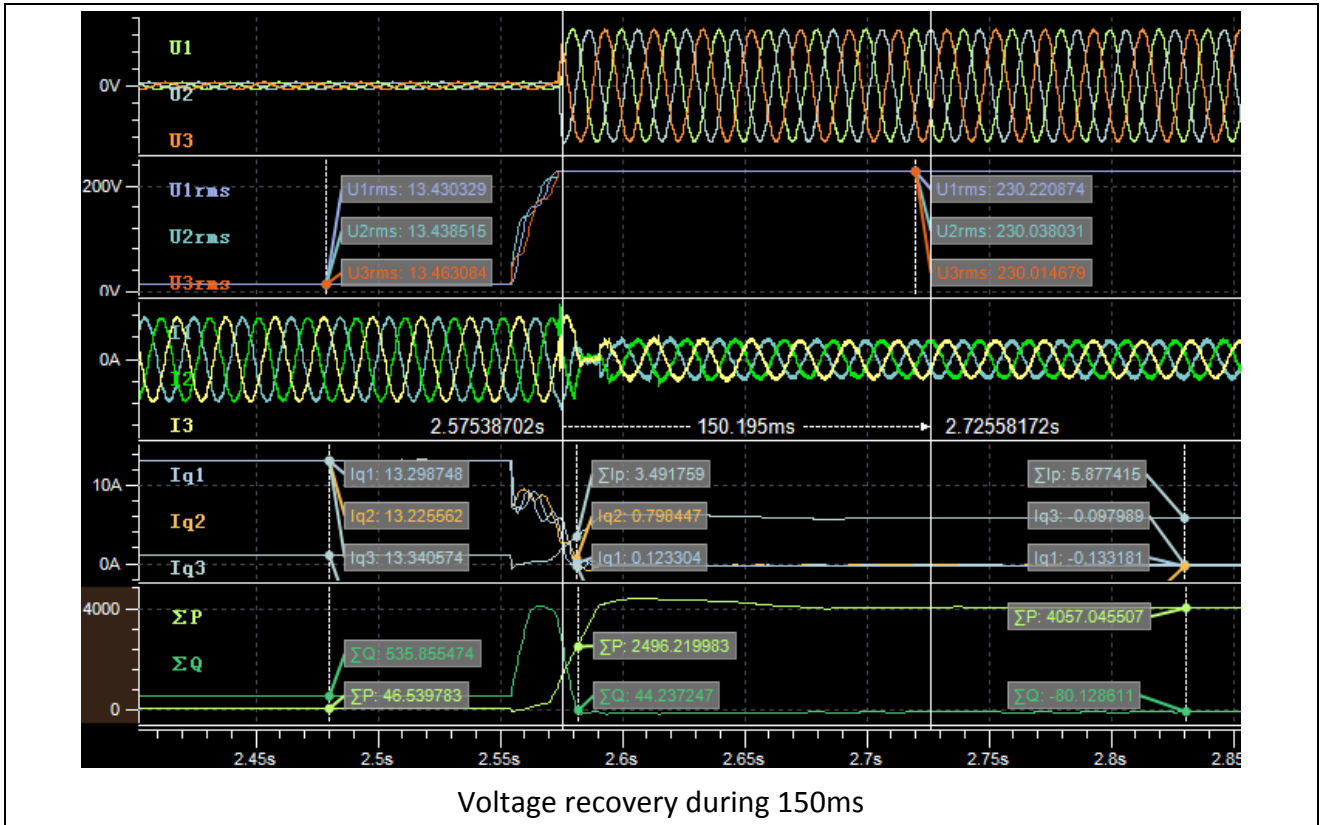
Graph_Phase C



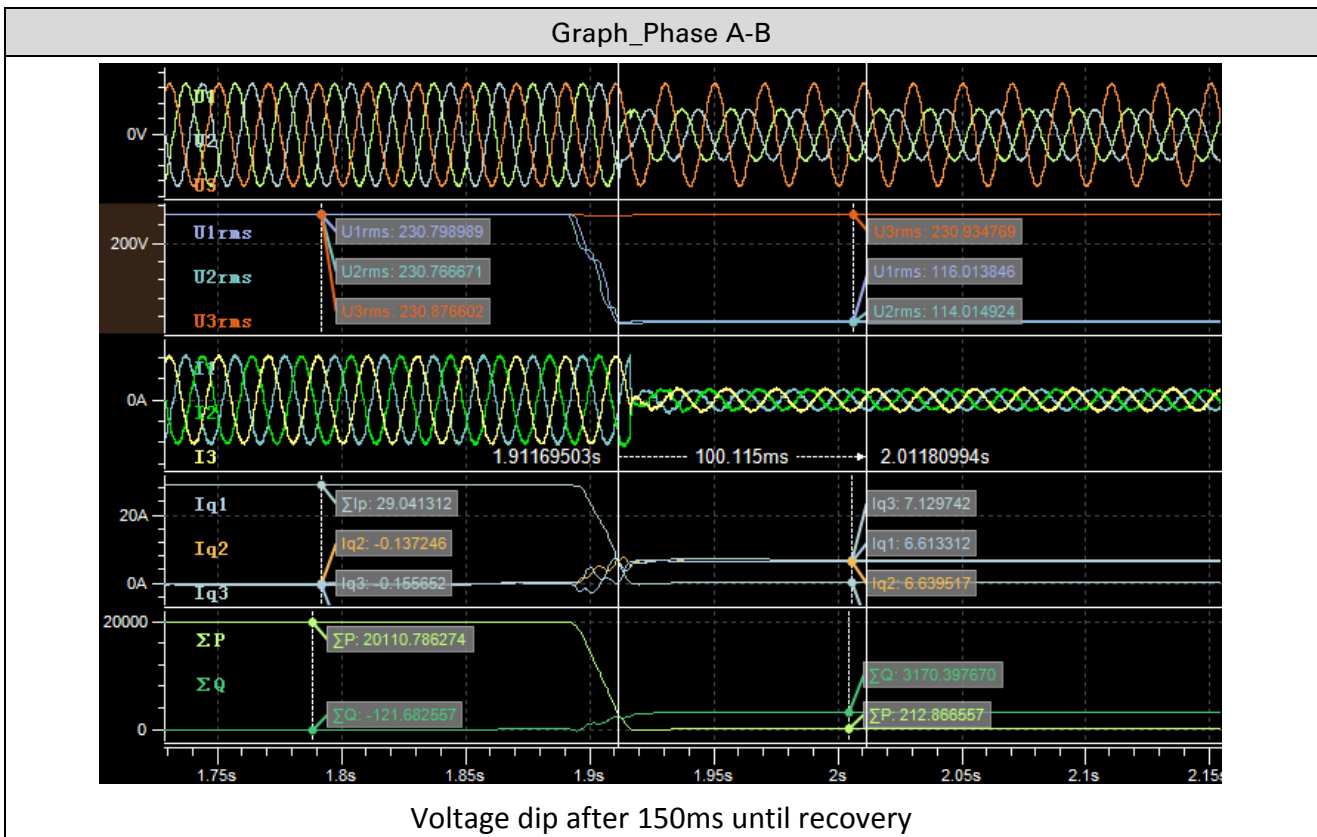
Voltage dip and during 150ms



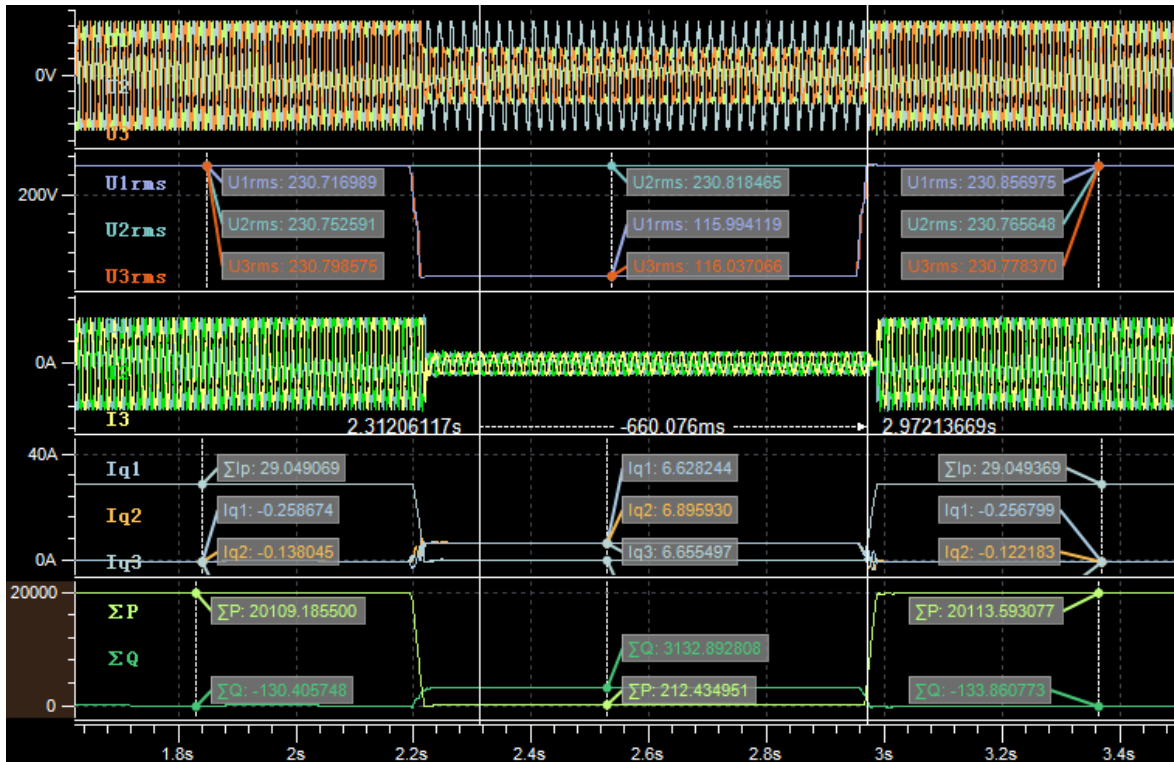
Voltage dip after 150ms until recovery



Behaviour during grid disturbance				
Unbalanced faults				
Test No.2.3				
Voltage dip	Measurement			Limit
	Phase A-B	Phase A-C	Phase B-C	
Voltage dip after 150ms until recovery				
Net reactive consumption energy $E_r < 40\%P_n * 100ms$	15.83 ms*p.u	15.66 ms*p.u	15.79 ms*p.u	-40ms*p.u
Net reactive consumption $Q < 40\%P_n(20ms)$	0.1583p.u	0.1566p.u	0.1579p.u	-0.4 p.u
Net active power consumption energy $E_p < 45\%P_n * 100ms$	1.050 ms*p.u	1.062 ms*p.u	1.031 ms*p.u	-45ms*p.u
Net active power consumption $P < 30\%P_n(20ms)$	0.0105p.u	0.0106p.u	0.0103p.u	-0.3 p.u

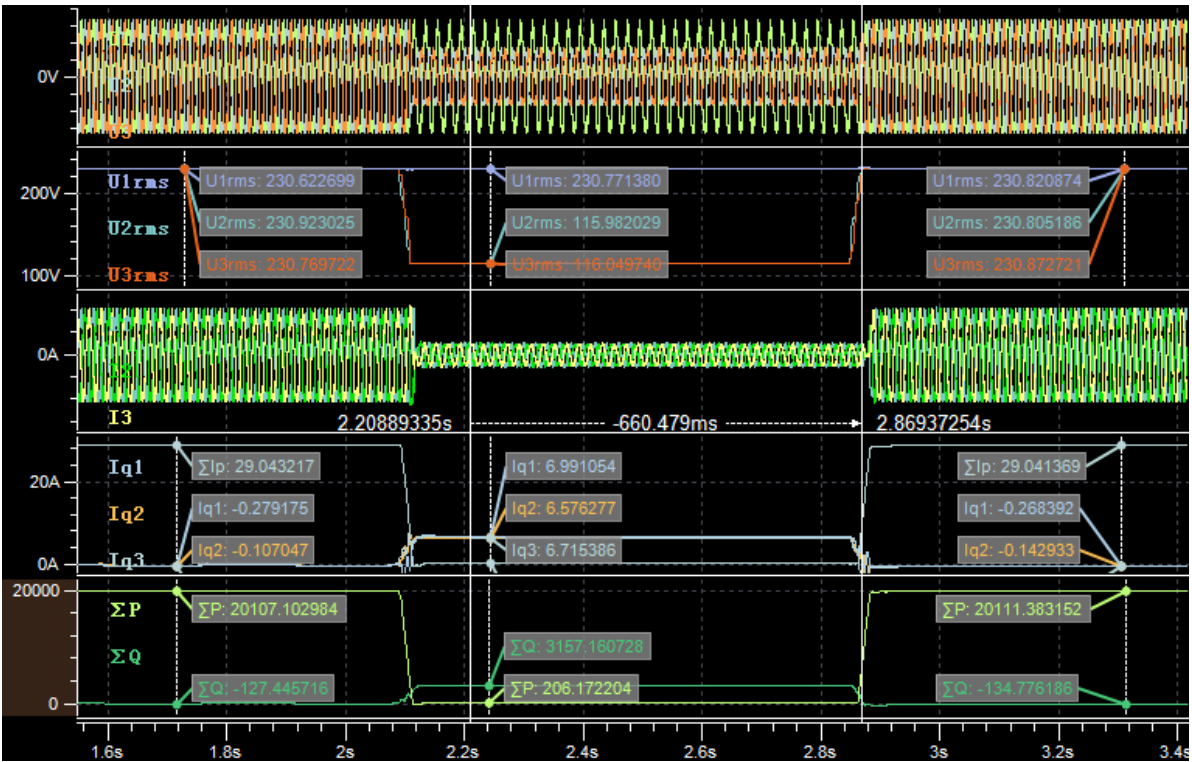


Graph_Phase A-C



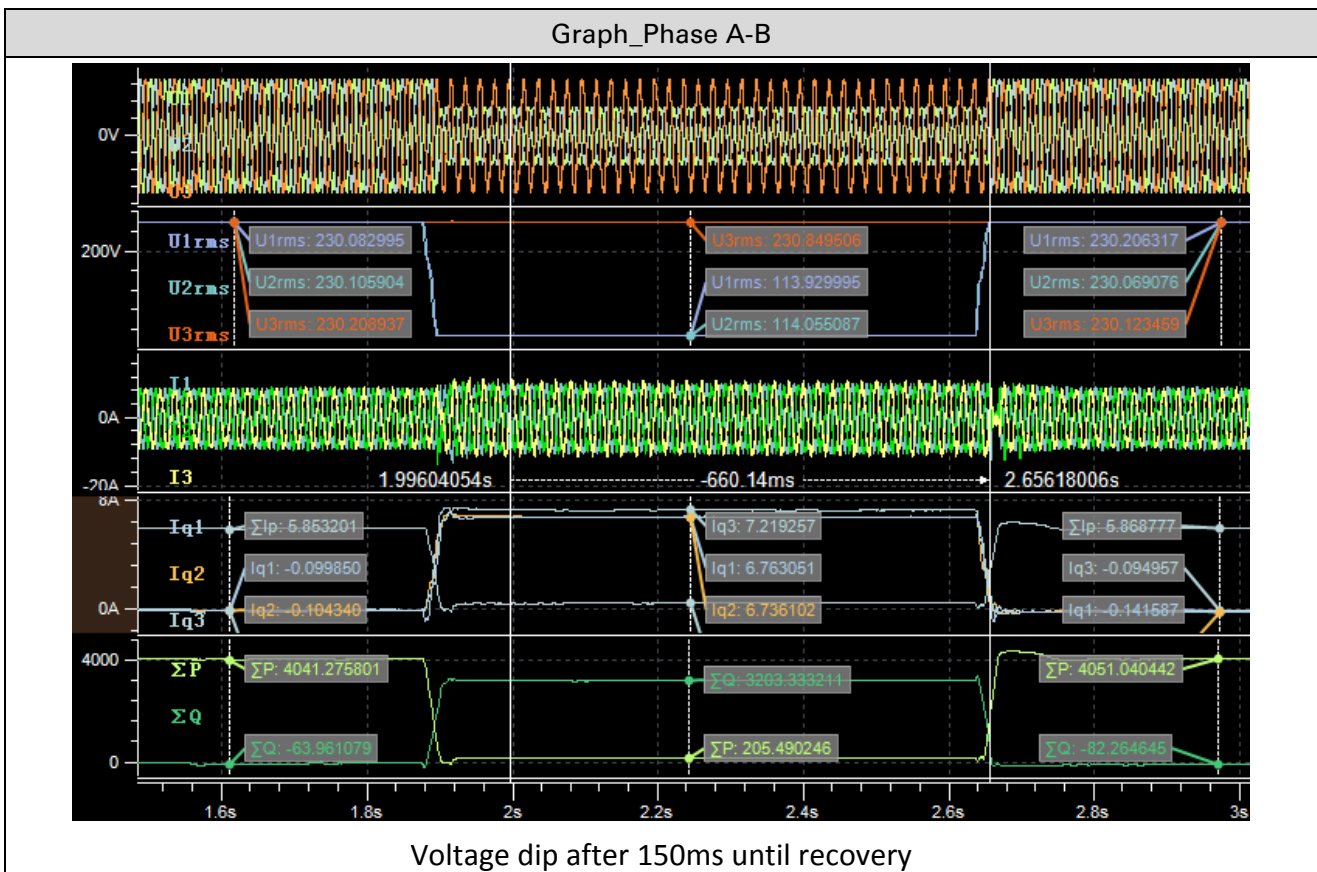
Voltage dip after 150ms until recovery

Graph_Phase B-C

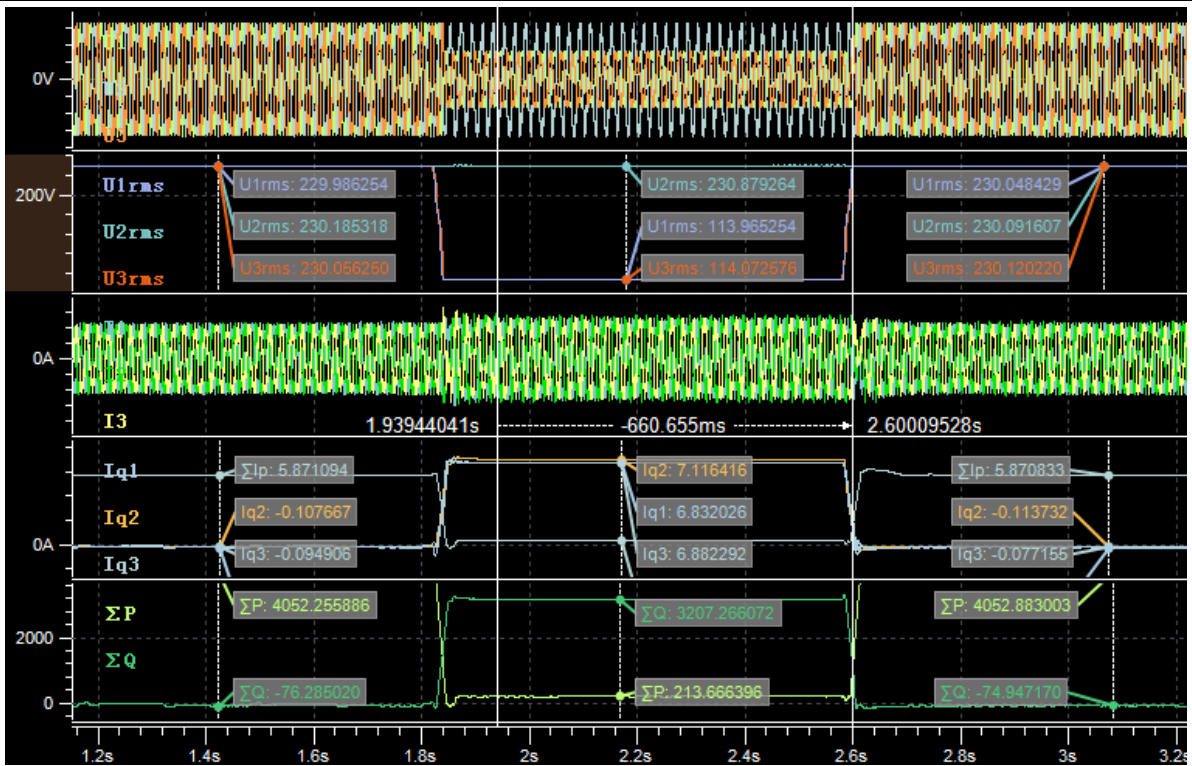


Voltage dip after 150ms until recovery

Behaviour during grid disturbance				
Unbalanced faults				
Test No.2.4				
Voltage dip	Measurement			Limit
	Phase A-B	Phase A-C	Phase B-C	
Voltage dip after 150ms until recovery				
Net consumption energy $E_{r < 40\% P_n} * 100ms$	16.017 ms*p.u	16.036 ms*p.u	16.107 ms*p.u	-40ms*p.u
Net consumption $Q < 40\% P_n(20ms)$	0.1602p.u	0.1604p.u	0.1611p.u	-0.4 p.u
Net consumption energy $E_{p < 45\% P_n} * 100ms$	1.030 ms*p.u	1.068 ms*p.u	1.020 ms*p.u	-45ms*p.u
Net consumption $P < 30\% P_n(20ms)$	0.0103p.u	0.0107p.u	0.0102p.u	-0.3 p.u

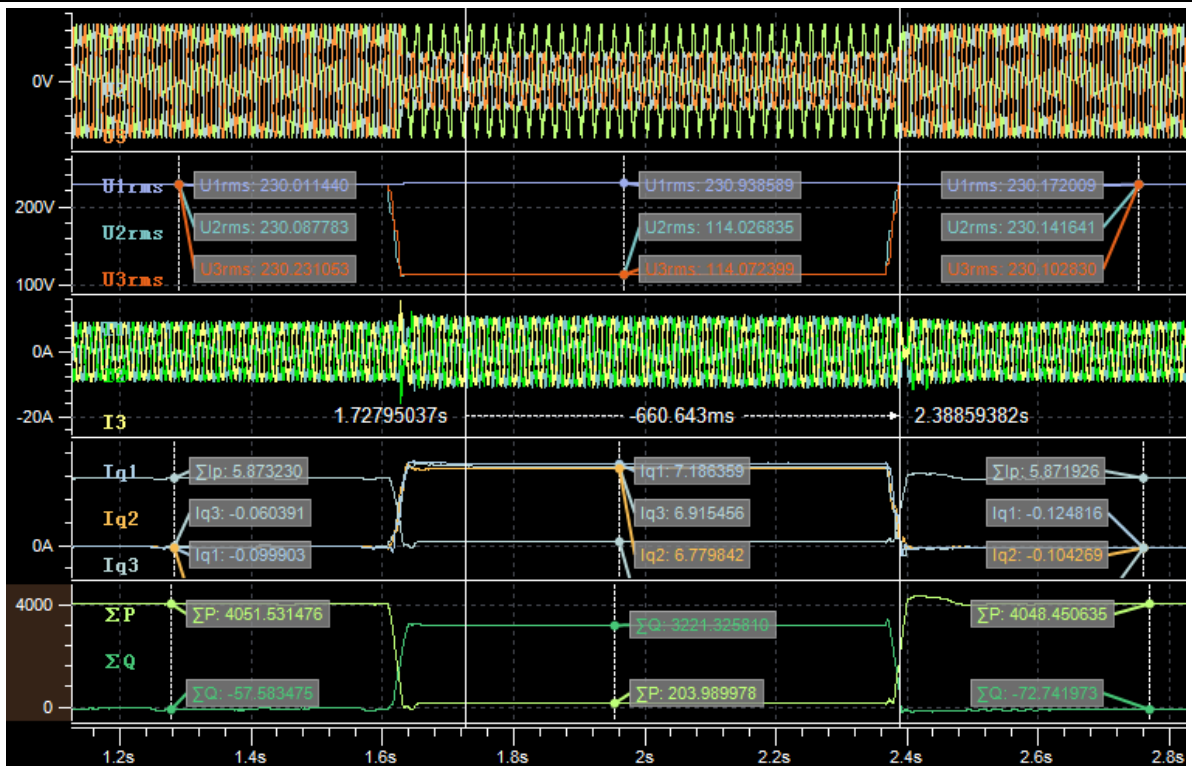


Graph_Phase A-C



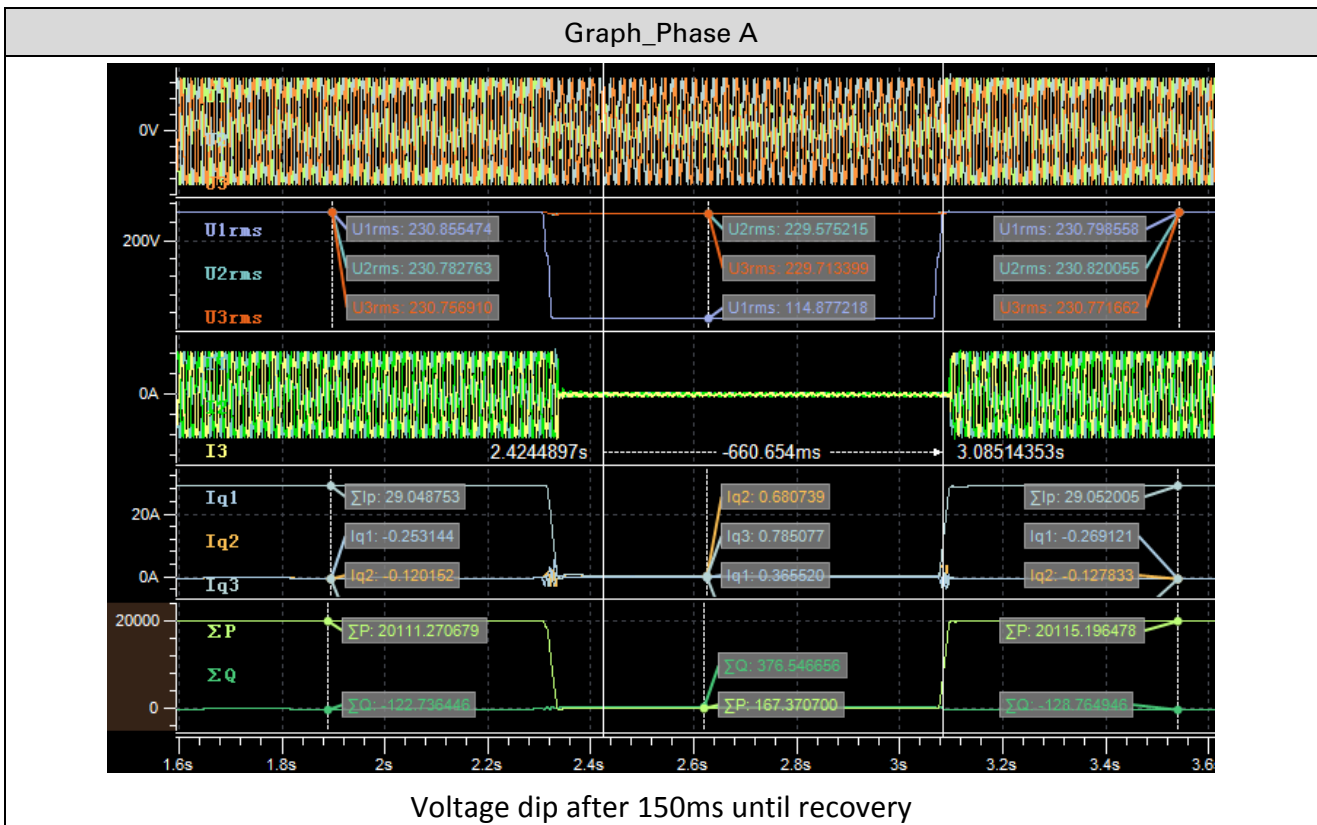
Voltage dip after 150ms until recovery

Graph_Phase B-C

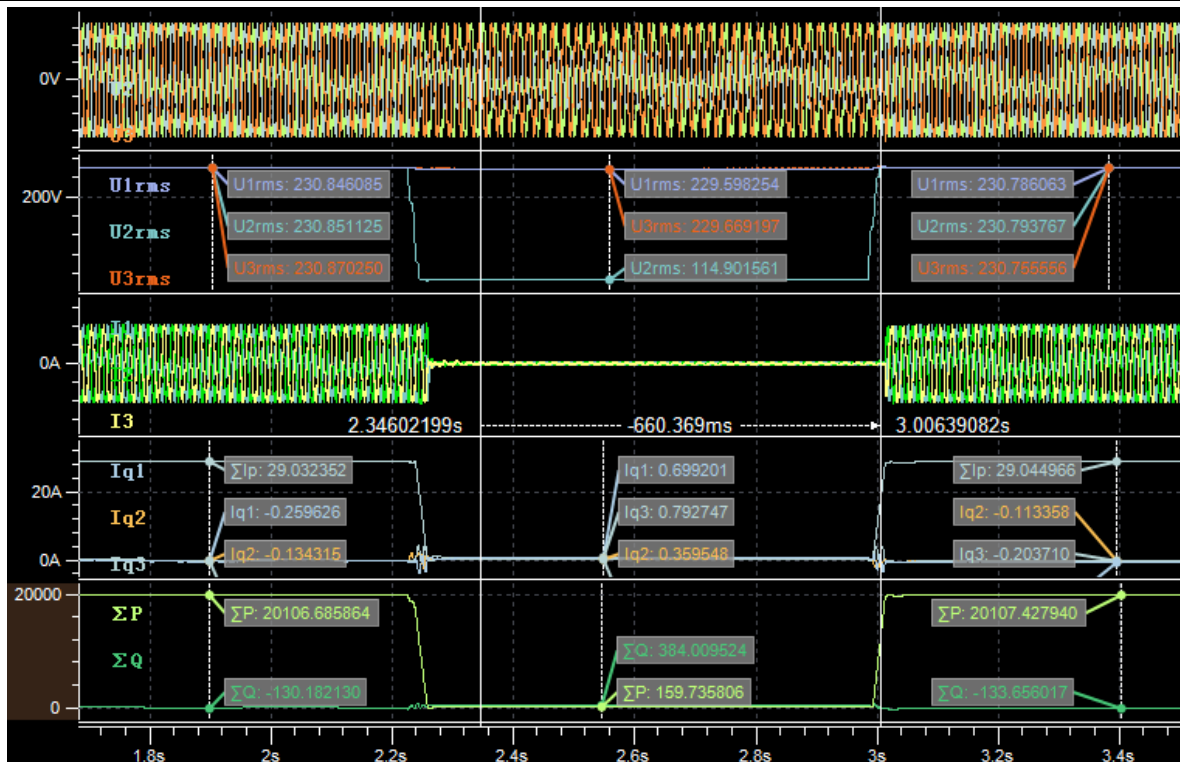


Voltage dip after 150ms until recovery

Behaviour during grid disturbance				
Unbalanced faults				
Test No.2.5				
Voltage dip	Measurement			Limit
	Phase A	Phase B	Phase C	
Voltage dip after 150ms until recovery				
Net ractive consumption energy $E_r < 40\%P_n * 100ms$	1.883 ms*p.u	1.920 ms*p.u	1.967 ms*p.u	-40ms*p.u
Net ractive consumption $Q < 40\%P_n(20ms)$	0.0188p.u	0.0192p.u	0.0197p.u	-0.4 p.u
Net active power consumption energy $E_p < 45\%P_n * 100ms$	0.837 ms*p.u	0.799 ms*p.u	0.821 ms*p.u	-45ms*p.u
Net active power consumption $P < 30\%P_n(20ms)$	0.0084p.u	0.0080p.u	0.0082p.u	-0.3 p.u

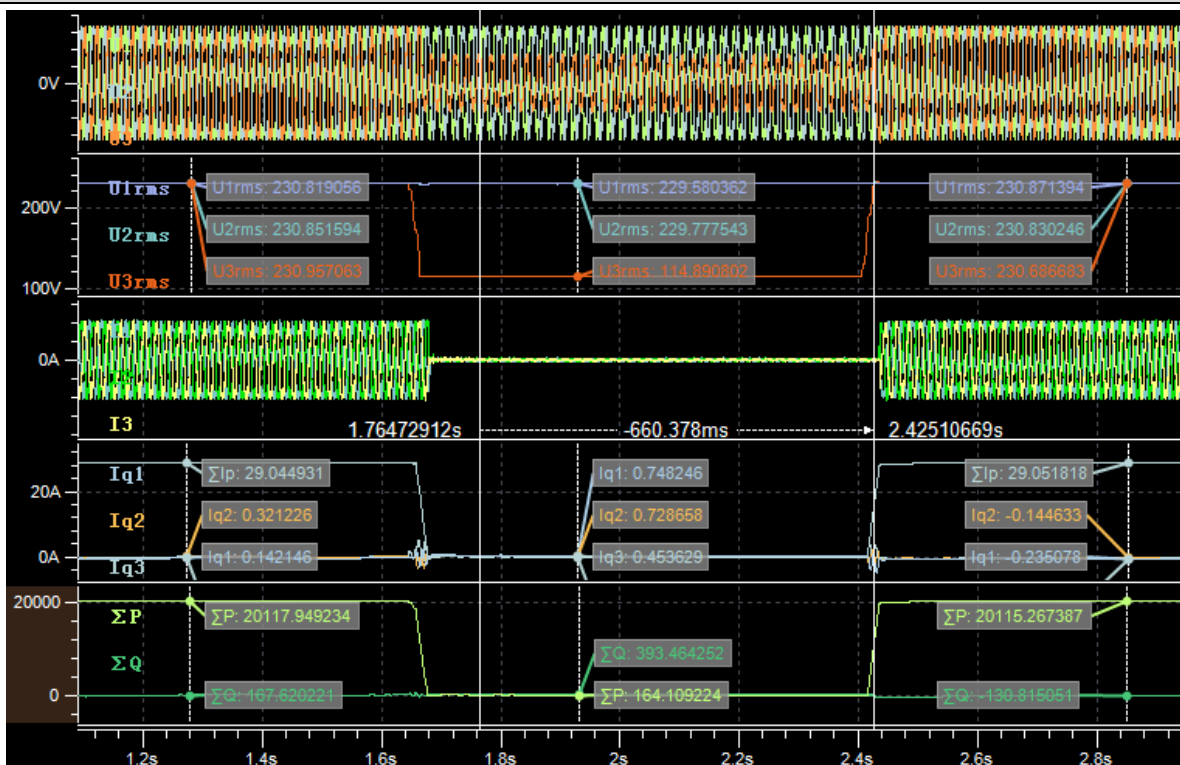


Graph_Phase B



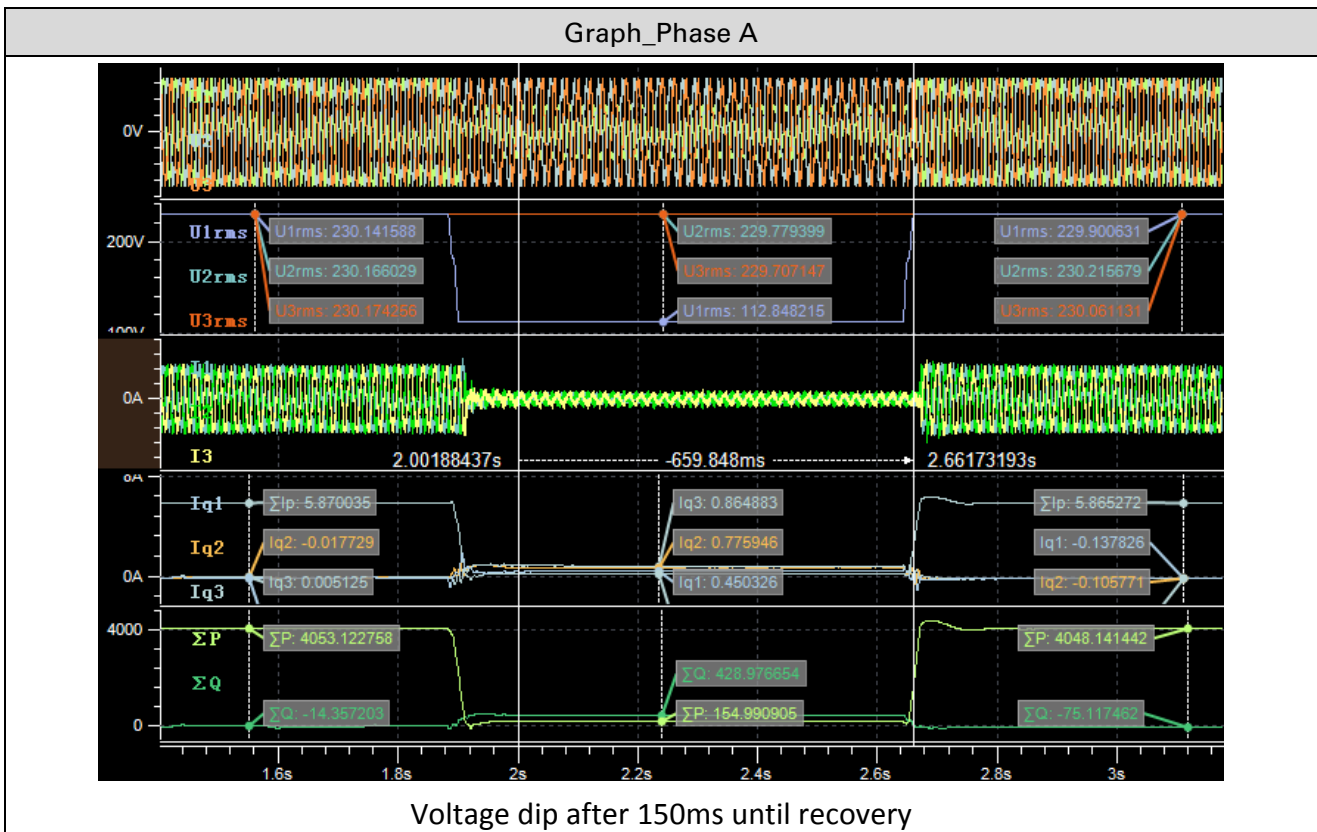
Voltage dip after 150ms until recovery

Graph_Phase C

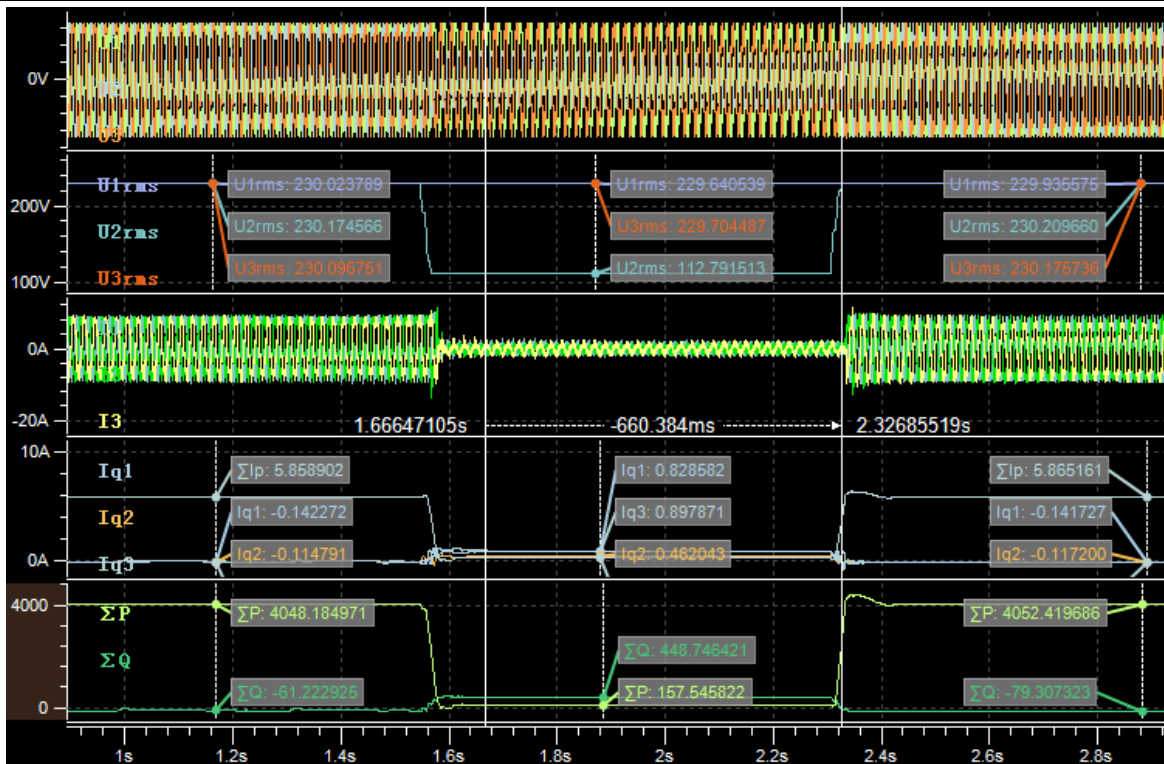


Voltage dip after 150ms until recovery

Behaviour during grid disturbance				
Unbalanced faults				
Test No.2.6				
Voltage dip	Measurement			Limit
	Phase A	Phase B	Phase C	
Voltage dip after 150ms until recovery				
Net reactive consumption energy $E_r < 40\%P_n * 100ms$	2.145 ms*p.u	2.244 ms*p.u	2.256 ms*p.u	-40ms*p.u
Net reactive consumption $Q < 40\%P_n(20ms)$	0.0215p.u	0.0224p.u	0.0226p.u	-0.4 p.u
Net active power consumption energy $E_p < 45\%P_n * 100ms$	0.775 ms*p.u	0.788 ms*p.u	0.806 ms*p.u	-45ms*p.u
Net active power consumption $P < 30\%P_n(20ms)$	0.0077p.u	0.0079p.u	0.0081p.u	-0.3 p.u

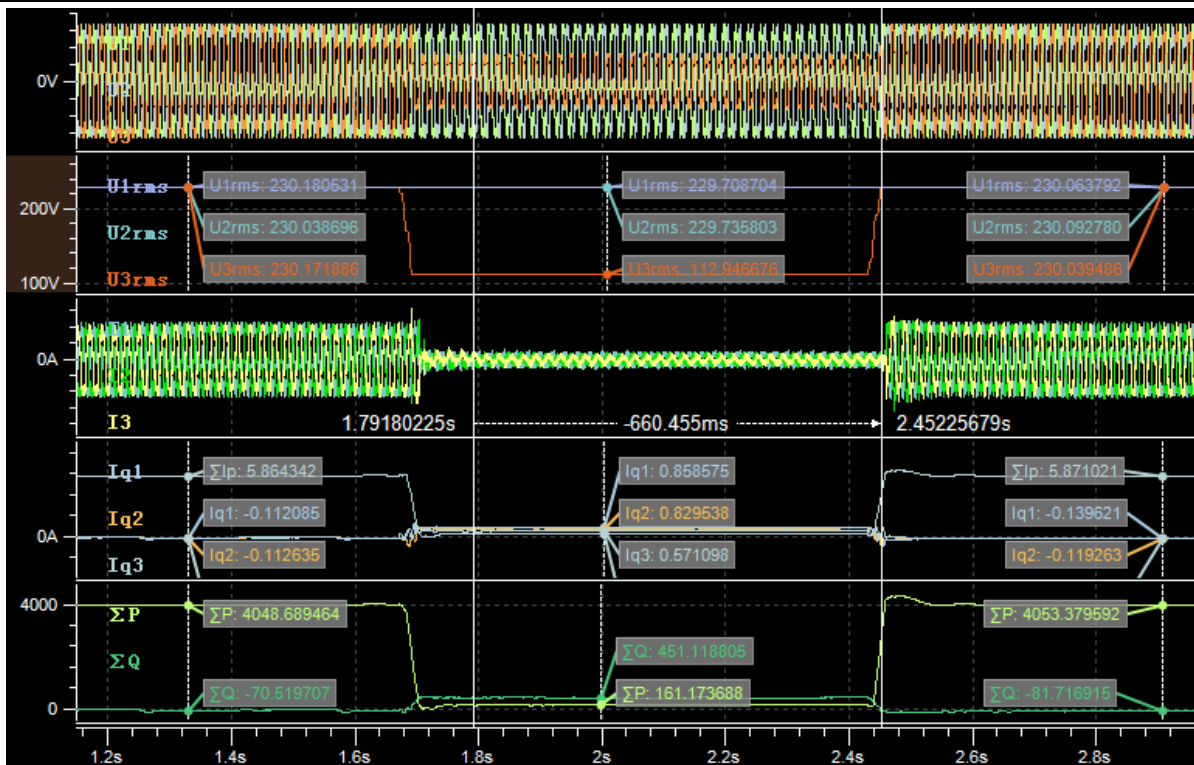


Graph_Phase B



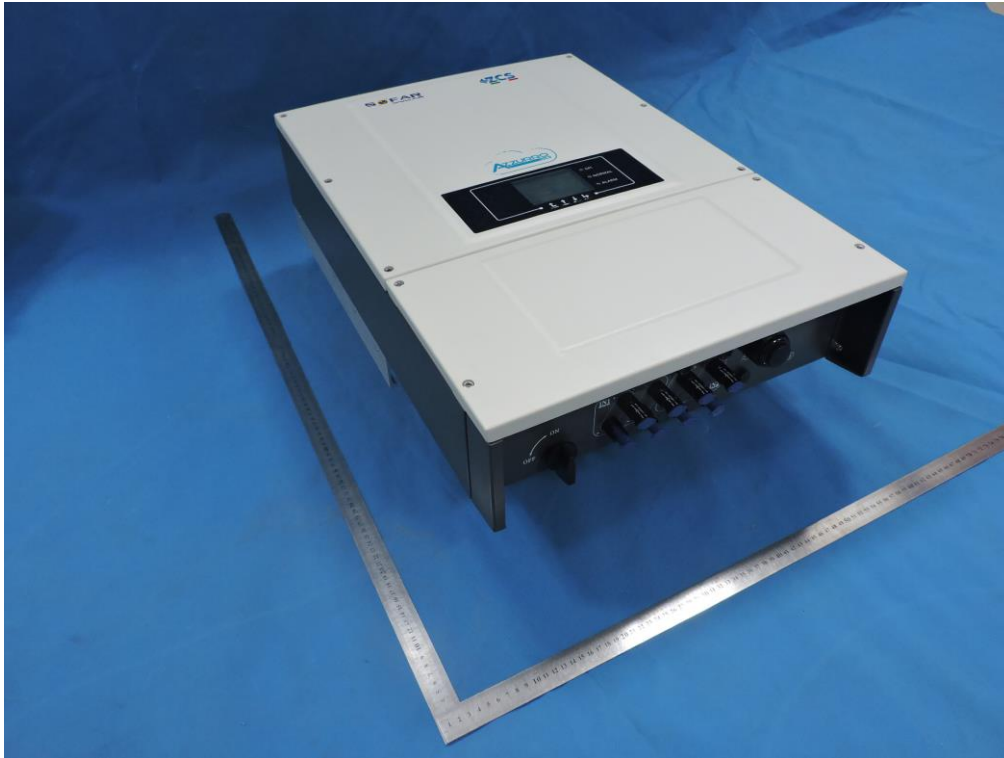
Voltage dip after 150ms until recovery

Graph_Phase C



Voltage dip after 150ms until recovery

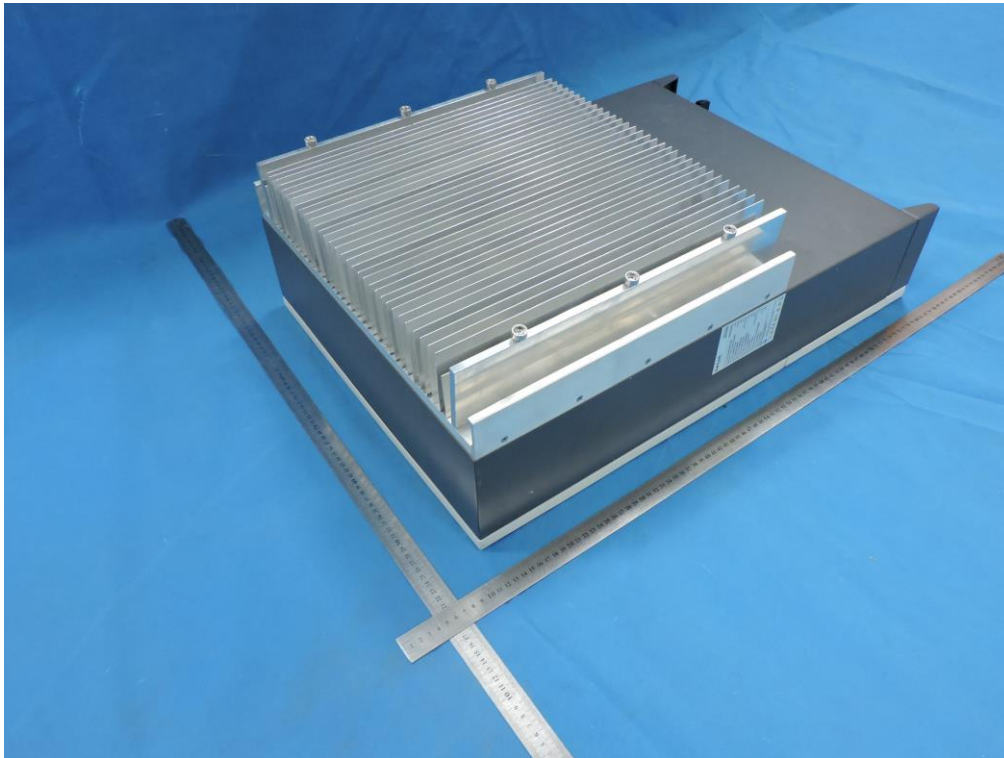
Appended photos



Overview



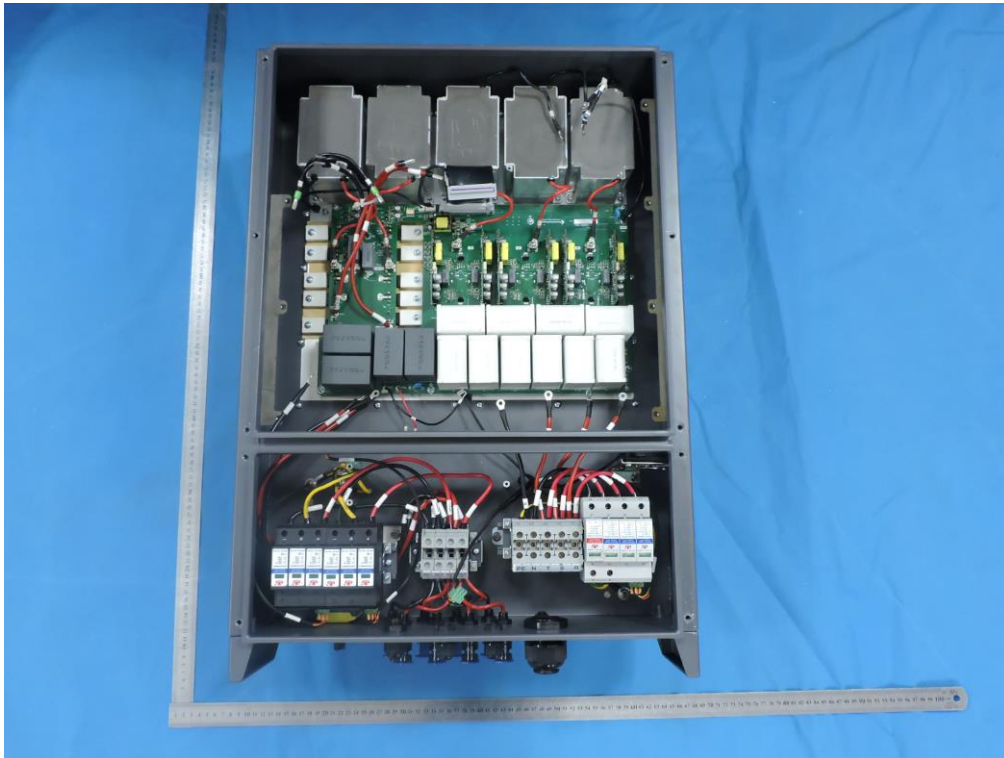
View of terminal



Rear view



Internal view



Internal view
(End of Report)